Buck Converters Using The *TOPSwitch®* Family

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Indroduction

The use of the highly integrated power conversion IC *TOPSwitch* from Power Integrations in isolated flyback switching power supplies is well known and documented in the comprehensive company literature. Because of its unique flexibility, *TOPSwitch* can also be used in a forward, boost or buck configuration. The following paper describes the buck topology in detail and provides the equations necessary for designing circuits using *TOPSwitch* in this configuration. As in off-line power supplies, the integration of a Power MOSFET together with a PWM control, the start-up circuit, and a current and overtemperature protection offers significant benefits for DC/DC converters, where an isolation is not required. Designers can build very compact and cost effective power supplies capable of dealing with wide input voltage ranges.

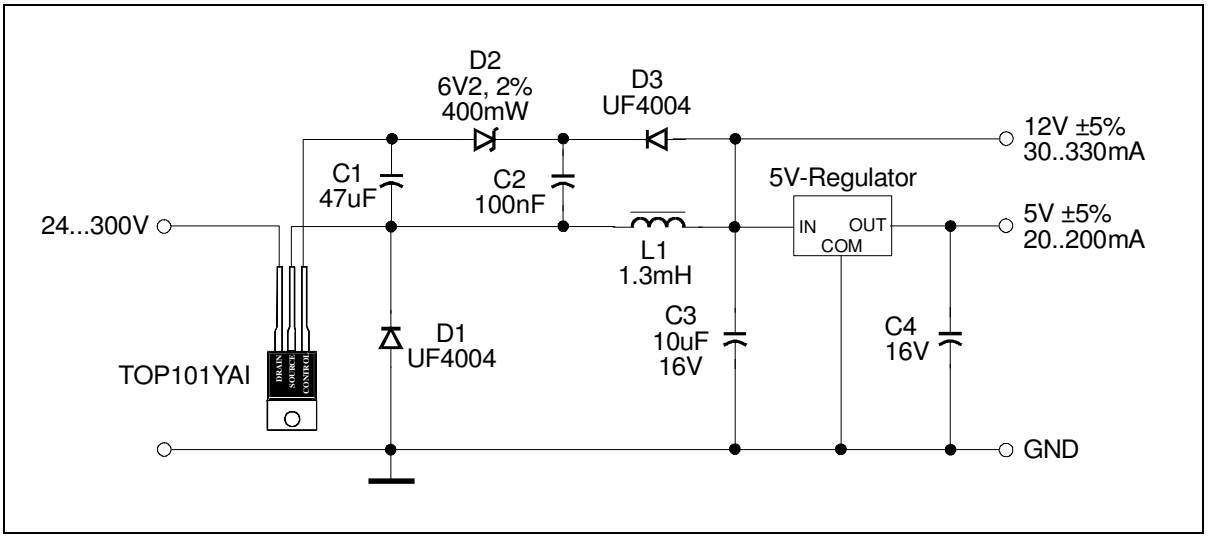


Figure 1. Basic buck converter with *TOPSwitch*

Basic Circuit

The buck converter shown in figure 1, with an input voltage range from 24V to 300V and two output voltages with a total output power of 5W represents the basic circuit. As in other topologies, the *TOPSwitch* operates here as power switch and PWM controller unit at the same time. A detailed description of the functionallaty of *TOPSwitch* can be found in the Data Book and Design Guide.

In the circuit shown in figure 1, the voltage across the inductor L1 is rectified and smoothed through D3 and C2 and supplies the internal logic in addition to providing the control loop feedback signal. D1 maintains current flow through the inductor during off-time of the *TOPSwitch* integrated MOSFET. When the input voltage is applied first, an internal current source within *TOPSwitch* charges C1. As soon as C1 reaches 5.8 volts relative to the *TOPSwitch* Source pin, *TOPSwitch* starts to switch. Initially, the internal logic and the gate drive is supplied through the energy stored in capacitor C1. In addition, this capacitor is used together with its ESR for control loop compensation. When the output voltage reaches its regulated value, the *TOPSwitch* supply current is derived from the feedback current through D2. The linear regulator is needed in order to realize the second 5V output, as the buck topology is - unlike the flyback topology - able to provide one output voltage only. The output voltage V_{OUT} is determined by the

regulated Control-Pin voltage V_C=5.8V and the zener voltage of D2.

$$V_{OUT} = V_C + V_{ZD2} \quad (1)$$

Hence the minimum possible output voltage in this circuit is 5.8V. If lower output voltages are required (5V for instance), one has to use a linear regulator or look at slightly different circuits introduced later on in this paper.

The limiting paramaters of the input voltage range are the breakdown voltage of the respective *TOPSwitch* as well as its minimum and maximum duty cycle specifications, *TOPSwitch* is able to switch on the MOSFET. In terms of the MOSFET, the maximum specified breakdown voltage is 350V for the TOP1xx family and 700V for the TOP2xx familiy. Regarding the minimum input voltage, *TOPSwitch* will start operating with drain voltages as low as 16V. In cases where the input voltage is lower than 36V, the user has to consider, that the *TOPSwitch* charging current for C1 during initial start-up decreases and hence, the turn-on delay of the output voltages increases. With a Control-Pin capacitor of 47uF and a drain voltage of 16V, the turn-on delay is typically 450msec. compared to 190msec. at a drain voltage of 36V or above.

The maximum duty cycle range of *TOPSwitch* is specified in the data sheet between 3% and 64%. The minimum and the maximum duty cycle, required in any particular design, is determined through the output voltage V_{OUT}, the forward voltage V_{FD1} of D1 and the saturation voltage V_{DS} of the MOSFET at the input voltage limits:

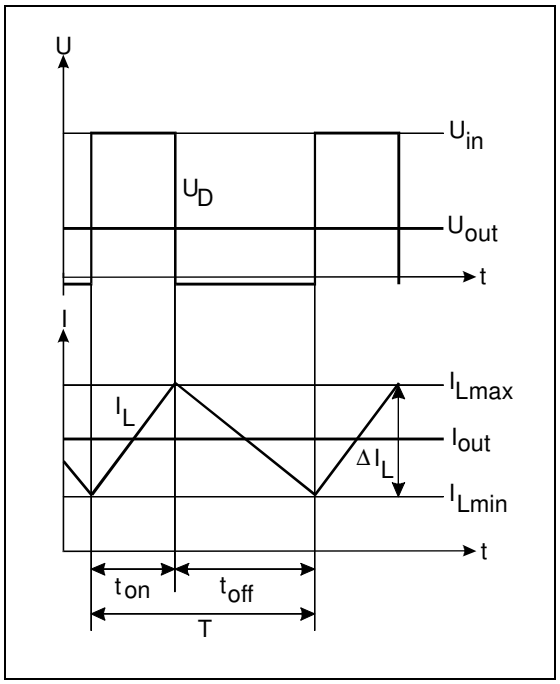
$$DC_{MIN} = \frac{V_{OUT} + V_{FD1}}{V_{IN,MAX} - V_{DS} + V_{FD1}} \quad (2)$$

$$DC_{MAX} = \frac{V_{OUT} + V_{FD1}}{V_{IN,MIN} - V_{DS} + V_{FD1}} \quad (3)$$

For the calculation of the inductor L1 figure 2 is quite useful showing qualitatively the voltage and current waveforms in a buck converter. In order to ensure, that during the switch-off time t_{OFF} of the integrated MOSFET, the voltage across the inductor does not drop to zero, the current continues flowing through the inductor. The condition for this continuous mode is as follows:

$$\Delta I_L \le 2 \cdot I_{OUT,MIN} \quad (4)$$

Figure 2. Voltage and current waveforms



$I_{OUT,MIN}$ is the sum of the minimum currents of both outputs. L_{MIN} is the minimum inductance necessary, in order to just get a continuous operation. Switching frequency f_{SW} of *TOPSwitch* is internally fixed and trimmed to 100kHz.

$$L_{MIN} = \frac{(V_{OUT} + V_{FD1}) \cdot (1 - DC_{MIN})}{f_{SW} \cdot \Delta I_L} \quad (5)$$

Thus, the real maximum current change ΔI_{LMAX} in L1, peak current I_{LMAX} through *TOPSwitch* and the inductor, and RMS current I_{LRMS} through L1 can be calculated with the selected value of L1 at DC_{MIN}:

$$\Delta I_{LMAX} = \frac{1}{L_1} \cdot (V_{OUT} + V_{FD1}) \cdot t_{OFF} \quad (6)$$

$$I_{LMAX} = I_{OUT} + \frac{\Delta I_{LMAX}}{2} \quad (7)$$

$$I_{LRMS} = \sqrt{I_{OUT}^2 + \left(\frac{\Delta I_L}{2 \cdot \sqrt{3}}\right)^2} \quad (8)$$

With an inductance of L1=1,3mH, as used in the example shown, the maximum current change in the inductor ΔI_{LMAX} is approximately 95mA. Hence from equation (7) and (8), I_{LMAX}=575mA and I_{LRMS}=530mA.

The current in inductor L1 has an AC and a DC component. The DC current is supplying the load and the AC current is flowing through capacitor C3. Thus this capacitance together with its ESR , determines the ripple voltage ΔU_{OUT}. The effective ESR can be decreased by adding a small ceramic capacitor in parallel to C3. V_{OUT} is the required output ripple voltage.

$$C_3 = \frac{\Delta I_{LMAX}}{8 \cdot f_{SW} \cdot \Delta V_{OUT}} \quad (9)$$

$$ESR_{C3} \leq \frac{\Delta V_{OUT}}{\Delta I_{LMAX}} \quad (10)$$

There are several methods to calculate the required core for the inductor L1. This paper details two techniques to determine the required core in more detail. The first considers the energy storage capability LI^2, and subsequently the core size is chosen from core data published by the manufacturer [2]. This energy storage capability is equal to:

$$LI_{LMAX}^2 = L_1 \cdot \left(I_{OUT} + \frac{\Delta I_{LMAX}}{2}\right)^2 \quad (11)$$

The second technique in choosing a suitable core is to determine the required effective magnetic core volume V_E:

$$V_E = \frac{I_{LMAX} \cdot L_1 \cdot \mu_e \cdot \mu_0}{B_{0MAX}^2} \quad (12)$$

B_{0MAX} is the magnetic saturation flux density of the core material, which can be found in the core databook and μ_e is the effective permeability. For toroidal chokes without airgap, this effective permeability μ_e can be calculated as:

$$\mu_e = \frac{1}{\mu_0} \cdot A_L \cdot \sum l/A \approx \mu_i \quad (13)$$

The specifications for the initial permeability μ_i, the inductance factor A_L and the magnetic core constant $\Sigma l/A$ can also be found in the core databook. Once a core is selected, the required turns in order to get the desired inductance L has to be calculated with the inductance factor A_L:

$$N = \sqrt{\frac{L_1}{A_L}} \quad (14)$$

For a switching frequency of 100kHz, the core material N67 [2] is suitable. The data sheet specifies the saturation flux density B_{0MAX}=510mT and the initial permeability μ_i=2300. Thus, from (12) the required magnetic core volume is V_E=8,3cm^3. The core size R36 offers a volume, closest to the calculated value. Made of the material N67, the inductance factor A_L is specified with 2300nH. Hence 24 turns are required for the desired inductance L_1=1,3mH.

The required wire diameter d is calculated with RMS current I_{LRMS} and the allowable current density S. Typical values in buck converters for S range from 3A/mm^2 to 8A/mm^2 [3]. With the high switching frequencies, the skin effect must be considered. Usually the relative resistance increase $R(f)/R_0$ due the skin effect should be lower than 5 to 6% [3].

$$d = 2 \cdot \sqrt{\frac{I_{LRMS}}{S \cdot \pi}} \quad (15)$$

$$d_{MAX} = 4 \cdot \frac{R(f)}{R_0} \cdot \sqrt{\frac{\sigma_{Cu}}{\pi \cdot f_{SW} \cdot \mu_0}} \quad (16)$$

In the example of figure 1, for a current density of S=5A/mm^2 the required wire diameter is 0,37mm. This value is safely below the maximum diameter of 0,89mm for an allowable resistance increase - caused by the skin effect - of 5%.

In the example circuit of figure 1, the tolerance of both output voltages is ±5%. For

the 12V output it's determined by the zener diode and the regulated control pin voltage V_C. By using a zener diode with a lower tolerance, 1% for instance, the regulation can be improved.

The diodes D1 and D3 should have a reverse recovery time t_{RR} lower than the *Leading Edge Blanking Time* of typical 150ns [3] of *TOPSwitch* in order to prevent premature termintion of the switching pulse. During this time, the internal current protection is deactivated on every switch-on cycle of the MOSFET in order to tolerate the unavoidable parasitc capacitive currents. Therefore reverse recovery times t_{RR} lower than 75ns are a practicable choice. Another criterion of the diode selection is the peak inverse voltage, which is applied at both diodes during switch-on of *TOPSwitch*. This peak inverse voltage is for D1 as high as the maximum input voltage and for D2 it's the difference between input and output voltage.

Second Circuit Example

Output voltages lower than the regulated control-pin voltage V_C=5.8V can be realized without an linear regulator by using an inexpensive opto-coupler. Figure 3 shows such an circuit.

The output voltage is determined by the zener voltage of D4, the voltage drop across R1 and the forward voltage drop of the opto-diode. D1 maintains current flow through the inductor during off-time of the integrated MOSFET. The voltage across the choke is rectified and smoothed through D1 and C2 in order to drive the opto-coupler. Zener diode D2 ensures that the voltage across the opto-transistor is lower than the breakdown voltage. Hence this diode has to be selected in accordance with the maximum input voltage and the opto-coupler rating.

The load regulation of this circuit as shown is approx. ±5% at load variations from 10 to 100%. This can be improved by using a zener diode with a tolerance of 1% or 2%. The same equations and rules demonstrated for the circuit of figure 1 can be used in order to determine the circuit parameters.

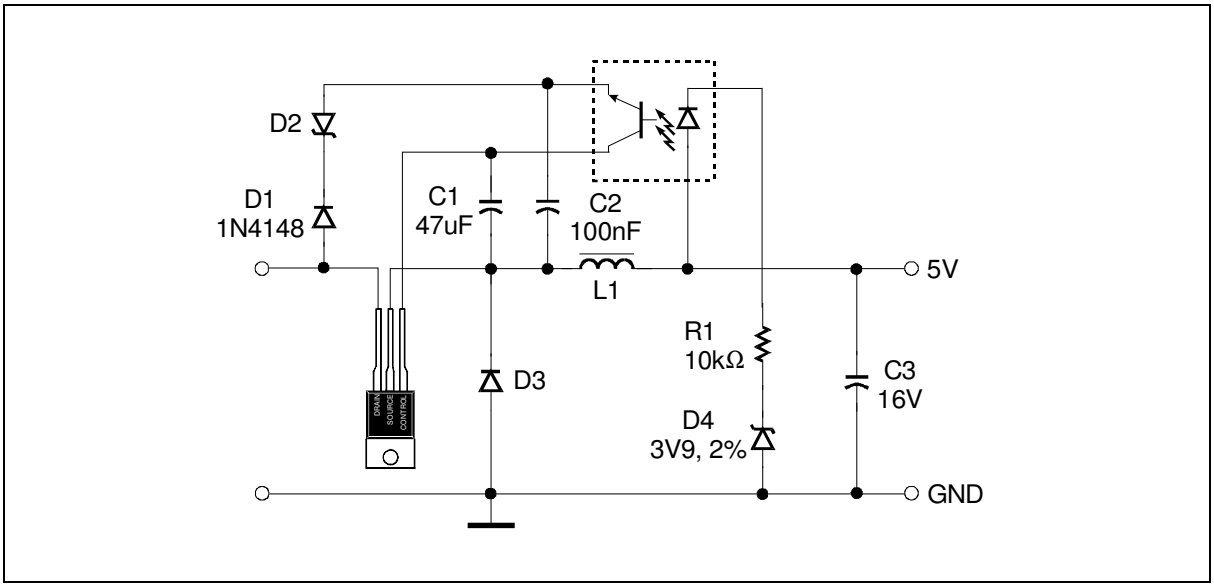


Figure 3. Buck Converter with TOPSwitch in an Opto-Coupler Configuration

Conclusion

This paper has demonstrated simple design procedures to provide low component count and cost effective buck converters using the *TOPSwitch* family. In addition to the familar flyback and boost converter topologies, the designer can now take advantage of the high level of integration offered by *TOPSwitch* in the buck configuration. Built-in current and temperature protection features, coupled with the integrated PWM control and switching MOSFET, yield very compact power supplies with the opportunity to design for an ultrawide input voltage range.

References

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