设计范例报告

标题	***参考设计报告：使用LinkSwitch™-HP LNK6774V设计的适用于LCD显示器的17 W双路输出反激式转换器***
规格	90 VAC – 265 VAC输入； 5 V, 1 A和18 V, 670 mA输出
应用	LCD显示器
作者	应用工程部
文档编号	RDR-321
日期	2012年9月28日
修订版本	2.2

特色概述

- 调整精度为±5%的初级侧稳压隔离反激式转换器
- 132 kHz开关频率可减小变压器及输出滤波器的尺寸。
- 满载连续导通模式工作可提高效率并降低输出电容纹波电流
- 多模式工作可提高整个负载范围内的效率
- 在230 VAC下，输入功率低于100 mW，负载待机功耗为50 mW
- 采用全面的保护功能，包括过压保护(OVP)、过热保护(OTP)、电压缓升/跌落保护、输入过压关断保护以及失稳压保护（自动重启动）
- 满足EN-550022和CISPR-22 Class B传导EMI要求
- 满足IEC61000-4-5的1 kV/2 kV浪涌电压要求

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目录

重要说明：
虽然本电路板的设计满足安全隔离要求，但工程原型尚未获得机构认证。因此，必须使用隔离变压器向原型板提供AC输入，以执行所有测试。

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1 简介

这份报告介绍的是一款采用LinkSwitch-HP系列IC器件LNK6774V设计的通用输入、5 V/1000 mA和18 V/670 mA隔离反激式转换器。它包含完整的电源规格、详细的电路原理图、构建电源所需的完整物料清单、详尽的电源变压器文档，以及测试数据和最重要的电气波形的波形图。

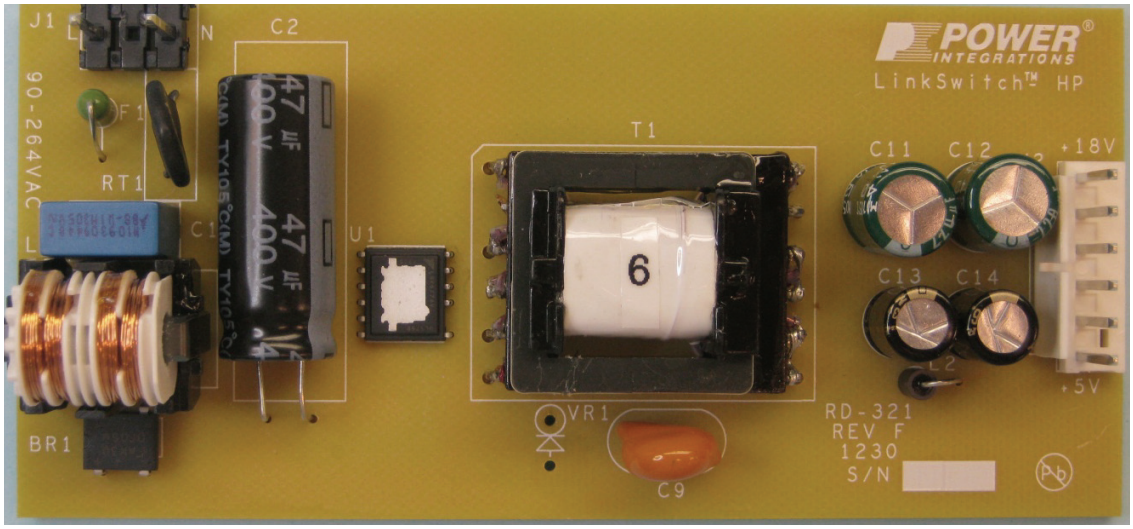

Figure 1 – Prototype Top View.

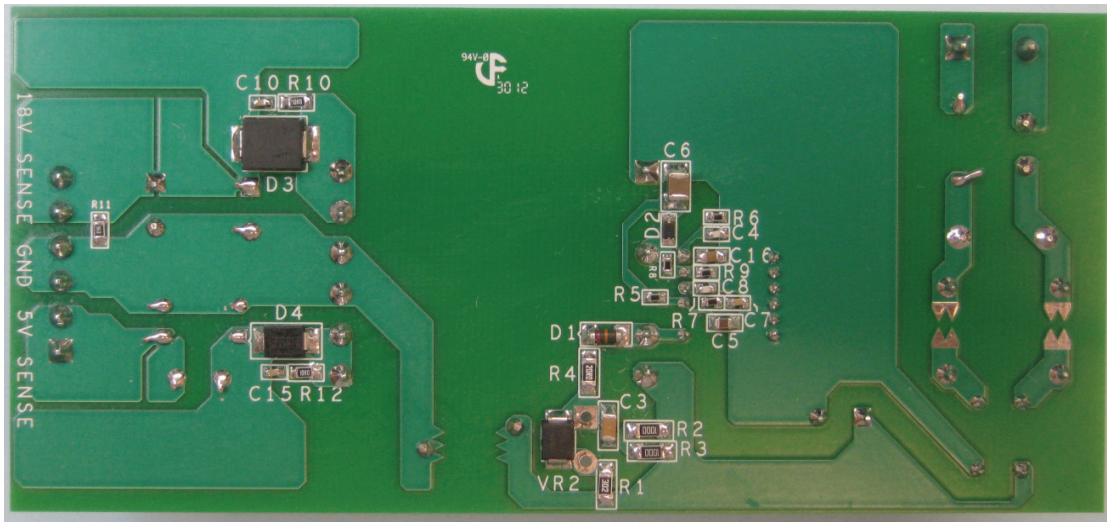

Figure 2 – Prototype Bottom View.

2 电源规格

下表所列为设计的最低可接受性能。实际性能可参考测量结果部分。

说明	符号	最小值	典型值	最大值	单位	备注
输入						
电压	V_{IN}	90		265	VAC	双导线 – 无P.E.
频率	f_{LINE}	47	50/60	64	Hz	
待机模式输入功率				100	mW	230 VAC，5 V 0.01 A， 18 V空载
输出						
输出电压1	V_{OUT1}	4.75	5	5.25	V	
输出纹波电压1	$V_{RIPPLE1}$			100	mVpp	20 MHz带宽， 稳态负载
输出电流1	I_{OUT1}	0.01		1500	mA	参见下面的负载间档
输出瞬态电压1	$V_{TRANSIENT1}$	4.75		5.5	V	参见下面的负载间档
输出电压2	V_{OUT2}	16.2	18	26	V	
输出纹波电压2	$V_{RIPPLE2}$				mV	20 MHz带宽
输出电流2	I_{OUT2}	0		670	mA	参见下面的负载间档
输出瞬态电压2	$V_{TRANSIENT2}$	16.2		28	V	参见下面的负载间档
总输出功率						
连续输出功率	P_{OUT}	0.05		17.1	W	
效率						
满载效率	η	80			%	90 VAC且满载
环境						
传导EMI		满足CISPR22B / EN55015B要求				
安全		其设计符合IEC950、UL1950 II类要求				
浪涌	DM	1			kV	1.2/50 μs浪涌，IEC 1000-4-5， 串联电阻： 差模：2 Ω 共模： 12 Ω
	CM	2				
ESD	**Air**	-15		15	kV	空气放电至输出连接器
	Contact	-6		6	kV	接触放电至输出连接器
环境温度	T_{AMB}	0		40	°C	自然对流，海平面

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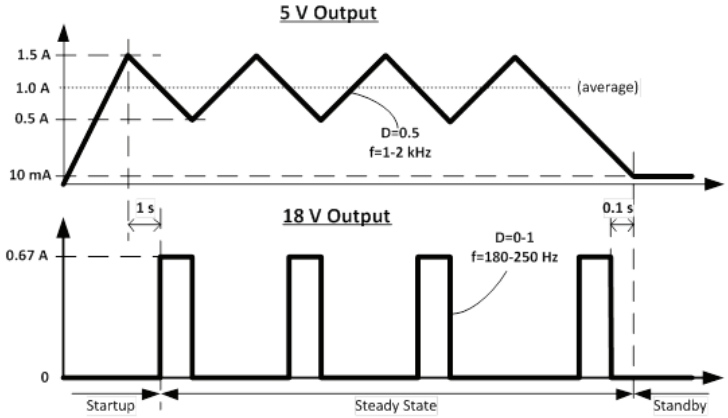

Figure 3 – Typical LCD Monitor Load Profile.

3 电路原理图

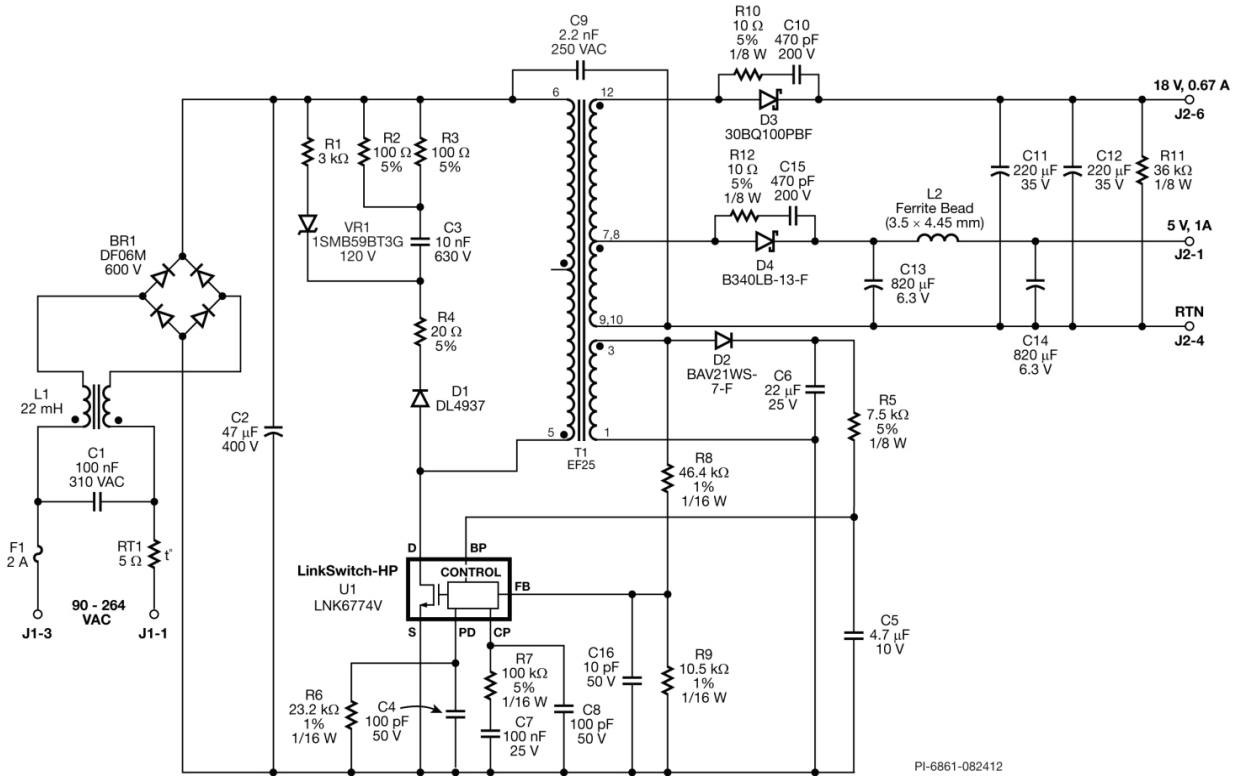

Figure 4 – Circuit Schematic.

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4 电路描述

4.1 输入整流和滤波

桥式整流管BR1对AC输入进行整流，C2对AC输入进行滤波。电感L1、C1和C2用于衰减差模和共模传导EMI。在构建变压器T1时采用了屏蔽技术(*E-Shield*™)，以降低共模EMI位移电流。这种滤波器设计、专有的E-Shield技术加上IC的频率抖动功能，为这种采用Y电容和初级侧RCD箝位电路的解决方案提供了出色的EMI性能。

4.2 LinkSwitch-HP初级

LNK6774V器件(U1)将振荡器、误差放大器和多模式控制电路、启动和保护电路以及高压功率MOSFET全部集成到了一个单片IC中。

电源变压器的一端连接到高压总线，另一端连接到U1的漏极引脚。在开关周期开始时，控制器将功率MOSFET导通，初级绕组中的电流不断增大，从而将能量存储在变压器磁芯中。当该电流达到内部误差放大器（CP引脚电压）设定的流限阈值时，控制器会关断功率MOSFET。由于变压器绕组需要调整相位和输出二极管需要调整方向，所存储的能量会在次级绕组中产生一个电压，这会对输出二极管进行正向偏置，然后将存储的能量传送到输出电容。

连接到旁路(BP)引脚的电容C5 (4.7 μF)将过压保护(OVP)、失稳压保护（自动重启动）和过热保护(OTP)设置为在给定关断期间（典型值为1500 ms）后尝试自动重启动。包括锁存OTP和OVP在内的其他组合可采用不同的电容值进行编程。如需进一步的详细信息，请参见LinkSwitch-HP数据手册。

4.3 初级RCD箝位

二极管D1、VR1、C3、R1、R2、R3和R4形成RCD缓冲电路，用于限制LinkSwitch-HP上的电压应力。峰值漏极电压在265VAC输入时可以控制在580V之下，对725V耐压(BV_{DSS})的MOSFET管来说有非常大的裕量。齐纳二极管VR1可防止电容C3在每个开关周期完全放电，从而降低待机工作时的功耗。

二极管D1、R2、VR1、C3、R5和R6形成RCD缓冲电路，用于限制LinkSwitch-HP上的电压应力。峰值漏极电压在265VAC输入时可以控制在580V之下，对700V耐压(BV_{DSS})的MOSFET管来说有非常大的裕量。

4.4 输出整流

对18 V输出的输出整流由二极管D3提供，滤波则由电容C11和C12提供。由R10和C10构成的缓冲电路提供高频率抖动，以提高EMI性能。对5 V输出的输出整流由二极管D4提供，滤波则由电容C13和C14以及电感L2提供。由R12和C15构成的缓冲电路提供高频率抖动，以提高EMI性能。

4.5 外部电流限流点设置

最大逐周期限流点由连接到PD引脚的电阻R6设定。本设计中采用了一个23.2 kΩ电阻，可将最大限流点设置到LNK6774V的默认限流点的60%。

4.6 反馈及补偿网络

输出电压通过偏置绕组和电阻分压器（R8和R9）在反激期间进行检测。检测到输出电压通过与FB引脚阈值进行比较来调整输出，或者在检测到过压时停止开关(OVP)。这种初级侧调节解决方案不仅能降低系统成本，还能延长系统的使用寿命，因为采用LinkSwitch-HP设计的电源无需使用光耦器（该元件可明显降低电源的寿命）。

分压器R8和R9还用于在集成的功率MOSFET导通期间间接监测总线电压。启动时，IC只会在总线电压通常达到100 V（电压缓升阈值）的情况下才开始开关。例如，当总线电压在电压跌落情况下降到40 V典型值以下时，器件将停止开关（电压跌落保护）。一旦总线电压达到过高水平（例如，由输入浪涌造成），器件将停止开关。此外，逐周期限流点还会在不同电压下得到补偿，以限制可用的过载功率。如需进一步的详细信息，请参见器件数据手册。

在FB引脚检测到的电压会在CP引脚产生控制电压。电阻R7以及电容C7和C8用于控制环路补偿。工作峰值初级电流和工作开关频率由CP引脚电压决定。

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5 PCB布局

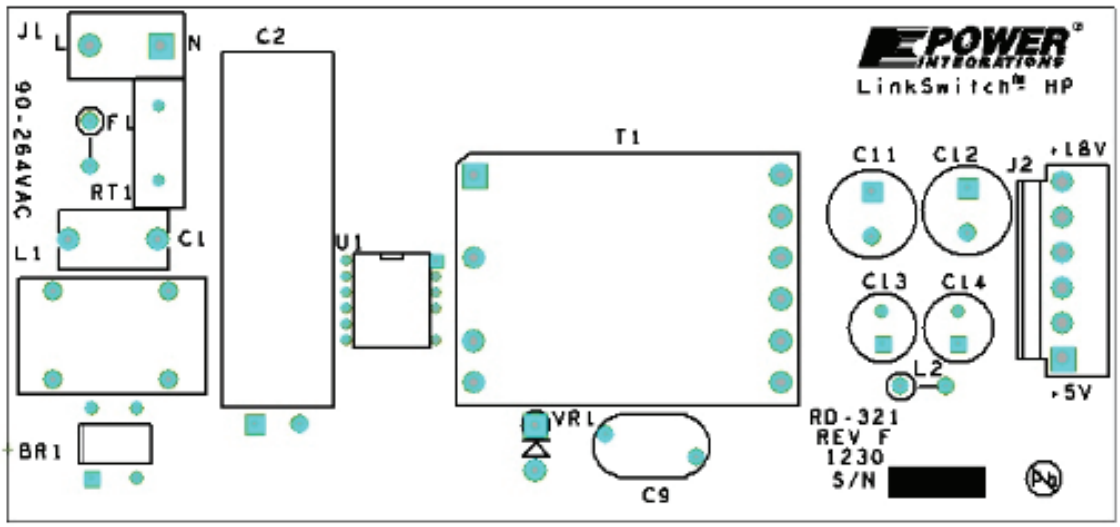

Figure 5 – PCB Top Side.

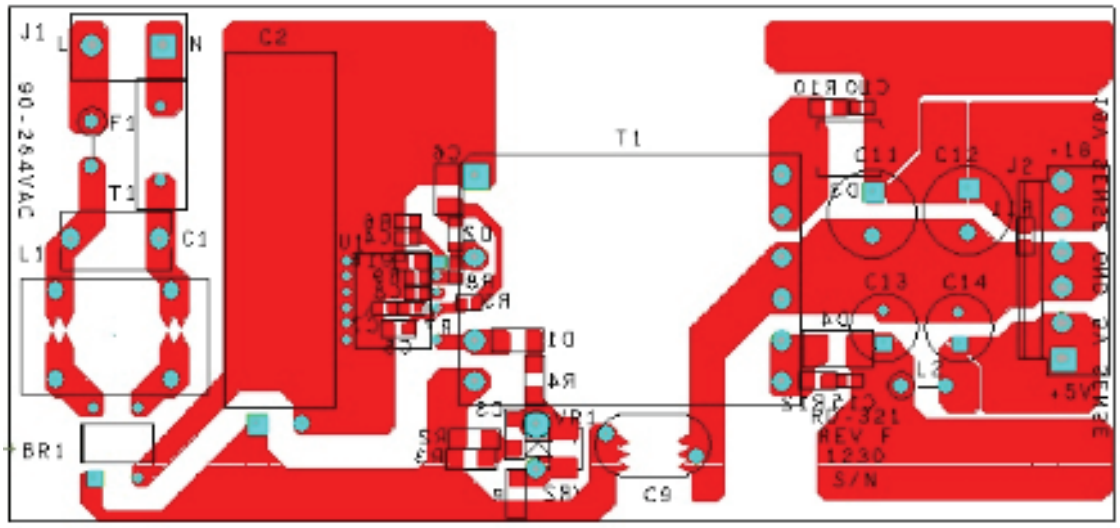

Figure 6 – PCB Bottom Side.

6 物料清单(BOM)

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 1 A, Bridge Rectifier, DFM package	DF06M	Diodes, Inc.
2	1	C1	100 nF, 310 VAC, Film, X2	B32921C3104M	Epcos
3	1	C2	47 μF, 400 V, Electrolytic, Low ESR, (12.5 x 30)	EPAG401ELL470MK30S	Nippon Chemi-Con
4	1	C3	10 nF, 630 V, Ceramic, X7R, 1206	C1206C103KBRACTU	Kemet
5	2	C4 C8	100 pF 50 V, Ceramic, NPO, 0603	CC0603JRNPO9BN101	Yageo
6	1	C5	4.7 μF, 10 V, Ceramic, X7R, 0805	C0805C475K8PACTU	Kemet
7	1	C6	22 μF, 25 V, Ceramic, X5R, 1210	ECJ-4YB1E226M	Panasonic
8	1	C7	100 nF, 25 V, Ceramic, X7R, 0603	VJ0603Y104KNXAO	Vishay
9	1	C9	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
10	2	C10 C15	470 pF, 200 V, Ceramic, X7R, 0603	06032C471KAT2A	AVX
11	2	C11 C12	220 μF, 35 V, Electrolytic, Very Low ESR, 53 mΩ, (10 x 12.5)	EKZE350ELL221MJC5S	Nippon Chemi-Con
12	2	C13 C14	820 μF, 6.3 V, Electrolytic, Low ESR, (8 x 11.5)	UHN0J821MPD	Nichicon
13	1	C16	10 pF, 50 V, Ceramic, NPO, 0805	ECJ-2VC1H100D	Panasonic
14	1	D1	600 V, 1 A, Rectifier, Fast Recovery, MELF (DL-41)	DL4937-13-F	Diodes, Inc.
15	1	D2	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
16	1	D3	100 V, 3 A, Schottky, SMC	30BQ100PBF	Vishay
17	1	D4	40 V, 3 A, Schottky, SMD, DO-214AA	B340LB-13-F	Diodes, Inc.
18	1	F1	Fuse, Pico, 2 A, 250 V, Fast, Axial	0263002.MXL	Littlefuse Inc.
19	1	J1	CONN HEADER 3POS (1x3).156 VERT TIN	26-64-4030	Molex
20	1	J2	CONN HEADER 6POS (1x6).156 VERT TIN	26-60-4060	Molex
21	1	L1	22 mH, 0.4 A, Common Mode Choke	ELF18D290C	Panasonic
22	1	L2	3.5 mm x 4.45 mm, 68 Ω at 100 MHz, #22 AWG hole, Ferrite Bead	2743001112	Fair-Rite
23	1	R1	3 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ302V	Panasonic
24	2	R2 R3	100 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ 101V	Panasonic
25	1	R4	20 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ 200V	Panasonic
26	1	R5	7.5 k Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3GEYJ 752V	Panasonic
27	1	R6	23.2 k Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2322V	Panasonic
28	1	R7	100 k Ω, 5%, 1/16 W, Thick Film, 0603	ERJ-3GEYJ 104V	Panasonic
29	1	R8	46.4 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4642V	Panasonic
30	1	R9	10.5 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1052V	Panasonic
31	2	R10 R12	10 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6 GEYJ100V	Panasonic
32	1	R11	36 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ363V	Panasonic
33	1	RT1	NTC Thermistor, 5 Ohms, 4.7 A	CL-150	Thermometrics
34	1	T1	Bobbin, EF25, Horizontal, 12 pins Transformer	YC2504 SNX-R1652	Ying Chin Santronics USA
35	1	U1	LinkSwitch-HP, eDIP-12P	LNK6774V	Power Integrations
36	1	VR1	120 V, 550 mW, 5%, SMB, 403A	1SMB59xxBT3G	Semiconductor
37	1	VR2	OPEN	OPEN	

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7 变压器设计表格

ACDC_LinkSwitch-HP_051612; Rev.0.13; Copyright Power Integrations 2012	INPUT	OUTPUT	UNIT	LinkSwitch-HP Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES				
VACMIN	90	90	V	Minimum AC Input Voltage
VACMAX	265	265	V	Maximum AC Input Voltage
fL	50	50	Hz	AC Mains Frequency
VO	5	5	V	Output Voltage (main)
PO	17	17	W	Output Power
n	0.82	0.82		Efficiency Estimate
Z	0.50	0.50		Loss Allocation Factor
VB	10	10	V	Bias Voltage
tC	3	3	ms	Bridge Rectifier Conduction Time Estimate
CIN	47	47	uF	Input Filter Capacitor
ENTER LINKSWITCH-HP VARIABLES				
LinkSwitch-HP	LNK6774V		LNK6774V	
ILIMITMIN		0.967	A	Minimum Current limit
ILIMITMAX		1.113	A	Maximum current limit
KI	0.60	0.600	A	Current limit reduction factor
ILIMITMIN_EXT			0.580	A
ILIMITMAX_EXT			0.668	A
fS		132000	Hz	LinkSwitch-HP Switching Frequency: Choose between 132 kHz and 66 kHz
fSmin		124000	Hz	LinkSwitch-HP Minimum Switching Frequency
fSmax		140000	Hz	LinkSwitch-HP Maximum Switching Frequency
KP	0.5	0.50		Ripple to Peak Current Ratio (0.4 < KP < 6.0)
VOR	110	110.00	V	Reflected Output Voltage
Voltage Sense				
VUVON			100	100.00
VUVOFF			42.55	V
VOV			446.26	V
FMAX_FULL_LOAD		132885	Hz	Maximum switching frequency at full load
FMIN_FULL_LOAD		117698	Hz	Minimum switching frequency at full load
TSAMPLE_FULL_LOAD				
TSAMPLE_LIGHT_LOAD		1.77	us	Minimum available Diode conduction time at light load. This should be greater than 1.11 us

Rpd		23.20	k-ohm	Program delay Resistor
Cpd	10	10.00	nF	Program delay Capacitor
Total programmed delay		0.06	sec	Total program delay
VDS		4.11	V	LinkSwitch-HP on-state Drain to Source Voltage
VD				
VDB			0.70	V
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES				
Core Type	EF25			
Core		EF25		Selected Core
Custom Core				Enter name of custom core is applicable
AE	0.5180	0.518	cm^2	Core Effective Cross Sectional Area
LE	5.7800	5.78	cm	Core Effective Path Length
AL	2000.0	2000	nH/T^2	Ungapped Core Effective Inductance
BW	15.6	15.6	mm	Bobbin Physical Winding Width
M	0.00	0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			4.00	4
NS	3.00	3		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS				
VMIN	85	85	V	Minmum DC Input Voltage
VMAX	375	375	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS				
DMAX		0.58		Maximum Duty Cycle
IAVG		0.24	A	
IP		0.56	A	Peak Primary Current
IR				
IRMS		0.33	A	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS				
LP_TYP		1436	uH	Typical Primary Inductance
LP_TOL	7	7	%	Primary inductance Tolerance
NP		60		Primary Winding Number of Turns
NB		6		Bias Winding Number of Turns
ALG		399	nH/T^2	Gapped Core Effective Inductance
BM		2607	Gauss	Maximum Flux Density at PO, VMIN (BM<3000)
BP		3301	Gauss	Peak Flux Density (BP<3700)
BAC		652	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)

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ur		1776		Relative Permeability of Ungapped Core
LG		0.13	mm	Gap Length (Lg > 0.1 mm)
BWE		62.4	mm	Effective Bobbin Width
OD	0.32	0.32	mm	Maximum Primary Wire Diameter including insulation
INS		0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.27	mm	Bare conductor diameter
AWG		30	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM				
CMA		310	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
FEEDBACK SENSING SECTION				
RFB1		37.40	k-ohms	Feedback divider upper resistor
RFB2				
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)				
Lumped parameters				
ISP		11.29	A	Peak Secondary Current
ISRMS		5.61	A	Secondary RMS Current
IO		3.40	A	Power Supply Output Current
IRIPPLE		4.46	A	Output Capacitor RMS Ripple Current
CMS		1122	Cmils	Secondary Bare Conductor minimum circular mils
AWGS		19	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS		0.91	mm	Secondary Minimum Bare Conductor Diameter
ODS				5.20
INSS		2.14	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS				
VDRAIN		626	V	Peak voltage acoss drain to source of Linkswitch-HP
PIVS		24	V	Output Rectifier Maximum Peak Inverse Voltage
PIVB				
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)				
1st output				
VO1	5.00	5	V	Output Voltage
IO1	1.00	1.00	A	Output DC Current
PO1		5.00	W	Output Power
VD1	0.35	0.35	V	Output Diode Forward Voltage Drop
NS1		2.92		Output Winding Number of Turns
ISRMS1		1.651	A	Output Winding RMS Current

IRIPPLE1		1.31	A	Output Capacitor RMS Ripple Current
PIVS1		23	V	Output Rectifier Maximum Peak Inverse Voltage
CMS1		330	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1		24	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1		0.51	mm	Minimum Bare Conductor Diameter
ODS1		5.35	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output				
VO2	18.00		V	Output Voltage
IO2	0.67		A	Output DC Current
PO2		12.06	W	Output Power
VD2	0.50	0.5	V	Output Diode Forward Voltage Drop
NS2		10.09		Output Winding Number of Turns
ISRMS2		1.106	A	Output Winding RMS Current
IRIPPLE2		0.88	A	Output Capacitor RMS Ripple Current
PIVS2		81	V	Output Rectifier Maximum Peak Inverse Voltage
CMS2		221	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2		26	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2		0.41	mm	Minimum Bare Conductor Diameter
ODS2		1.55	mm	Maximum Outside Diameter for Triple Insulated Wire

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8 变压器规格

8.1 电气原理图

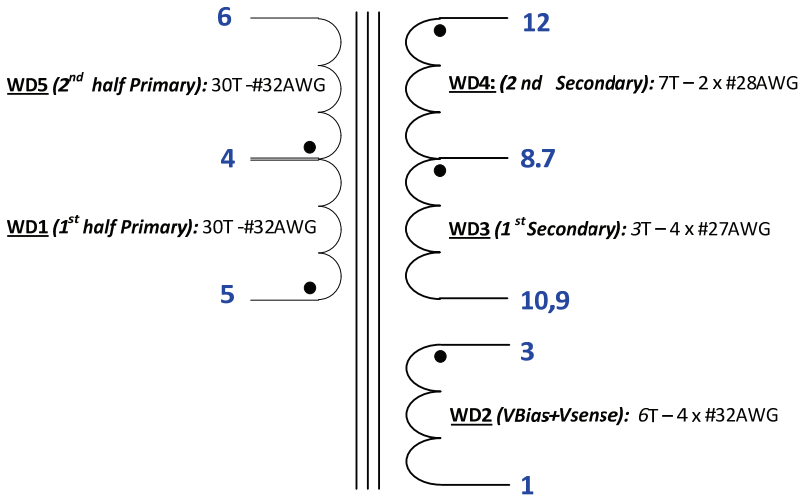

Figure 7 – Transformer Electrical Diagram.

8.2 电气规格

Electrical Strength	1 second, 60 Hz, from pins 1-6 and pins 7-12.	3000 VAC
Primary Inductance	Pins 5-6, all other windings open, measured at 100 kHz, 0.4 VRMS.	1436 µH ±7%
Resonant Frequency	Pins 5-6, all other windings open.	1500 kHz (Min.)
Primary Leakage Inductance	Pins 5-6, with pins 7-12 shorted, measured at 100 kHz, 0.4 VRMS.	15 µH (Max.)

8.3 材料

Item	Description
[1]	Core: EF25, TDK PC44-EF25Z, and gapped ALG 398.9 nH/T^2.
[2]	Bobbin: EF25-Horizontal, 12 pins (6/6), Ying Chin, P/N: YC-2504.
[3]	Magnet wire: #32 AWG Solderable, double coated.
[4]	Magnet wire: #27 AWG Solderable, double coated.
[5]	Magnet wire: #28 AWG Solderable, double coated.
[6]	Teflon tube: Alpha Wire, TFT, or equivalent.
[7]	Tape: 3M 44 Margin tape (cream), 3.5 mm wide, or equivalent.
[8]	Tape: 3M 1298 Polyester Film, 8.6 mm wide, 2.0 mils thick, or equivalent.
[9]	Tape: 3M 1298 Polyester Film, 15.6 mm wide, 2.0 mils thick, or equivalent.
[10]	Varnish: Dolph BC-359, or equivalent.

8.4 变压器结构图：

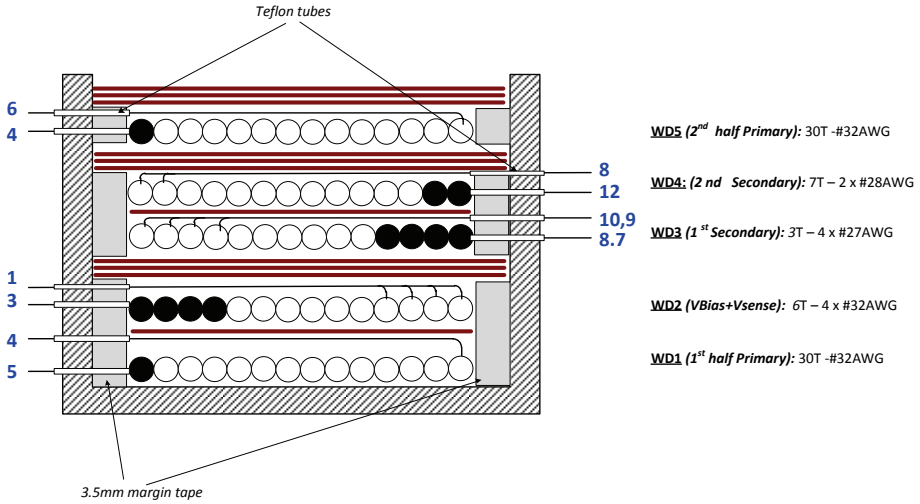

Figure 8 – Transformer Build Diagram.

8.5 变压器绕制：

Winding preparation	Place the bobbin item [2] on the mandrel with the primary side is on the left side. Winding direction is clockwise direction. Margin tape item [7] should be applied for all windings. Note: Teflon tubes item [6] should be inserted into all wire ends and reach to inside edge of margin tapes. Return wires should be inside the winding section and not overlap on the margin tape. (See pictures below).
WD1 1st Half Primary	Start at pin 5, wind 30 turns of wire item [3] from left to right with tight tension, at the last turn bring the wire back to the left, and terminate at pin 4.
Insulation	Place 1 layer of tape item [8].
WD2 VBias+VSense	Start at pin 3, wind 6 quad-filar turns of wire item [3] from left to right with tight tension, at the last turn bring the wire back to the left, and terminate at pin 1.
Insulation	Place 3 layers of tape item [9].
WD3 1st Secondary	Start at pins 8,7, wind 3 quad-filar turns of wire item [4] from right to left, spread the wire evenly, at the last turn bring the wire back to the right, and terminate at pin 10,9.
Insulation	Place 1 layer of tape item [8].
WD4 2nd Secondary	Start at pins 12, wind 7 bi-filar turns of wire item [5] from right to left, spread the wire evenly, at the last turn bring the wire back to the right, and terminate at pin 8.
Insulation	Place 3 layers of tape item [9].
WD5 2nd Half Primary	Start at pin 4, wind 30 turns of wire item [3] from left to right with tight tension, at the last turn bring the wire back to the left, and terminate at pin 6.
Final Assembly	Grind and secure core halves with tape. Vanish item [10].

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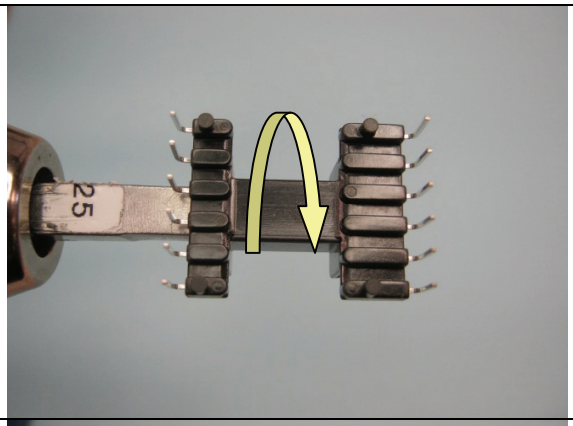
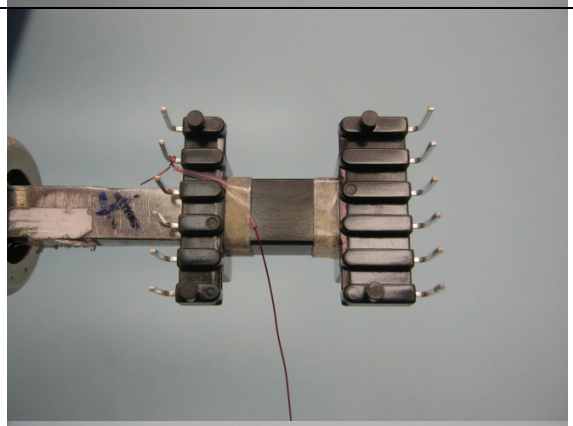
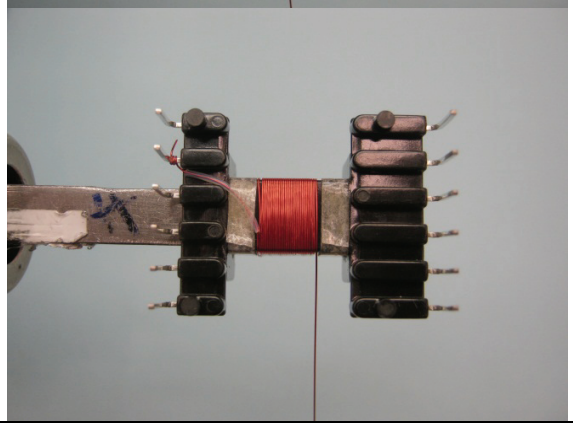
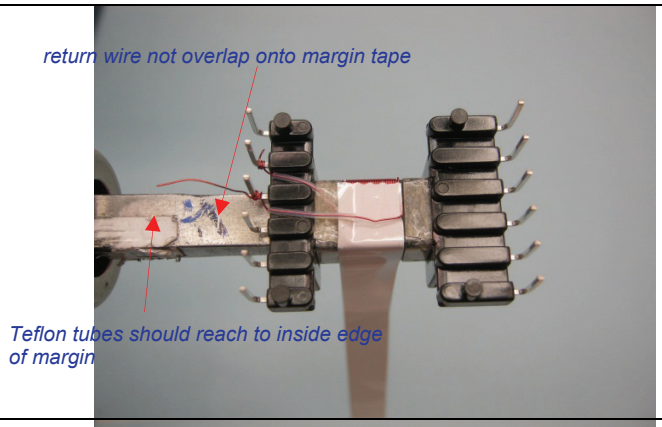
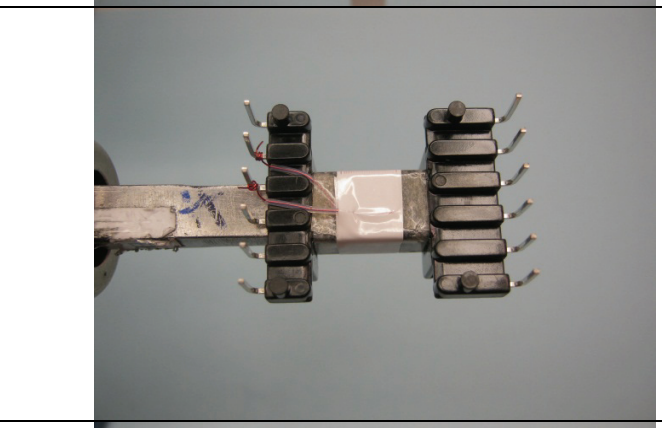
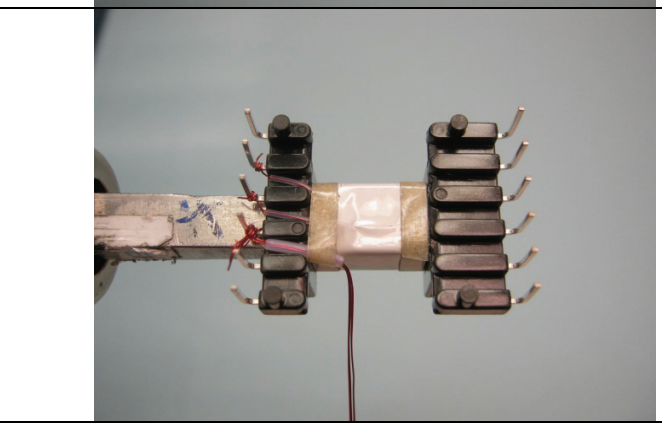
8.6 变压器绕制演示：

Winding Preparation			Place the bobbin item [2] on the mandrel with the primary-side is on the left side. Winding direction is clockwise direction.
WD1 1st Half Primary		 	Start at pin 5, wind 30 turns of wire item [3] from left to right with tight tension, at the last turn bring the wire back to the left, and terminate at pin 4.

			
Insulation			Place 1 layer of tape item [8].
WD2 VBias+VSense			Start at pin 3, wind 6 quad-filar turns of wire item [3] from left to right with tight tension,

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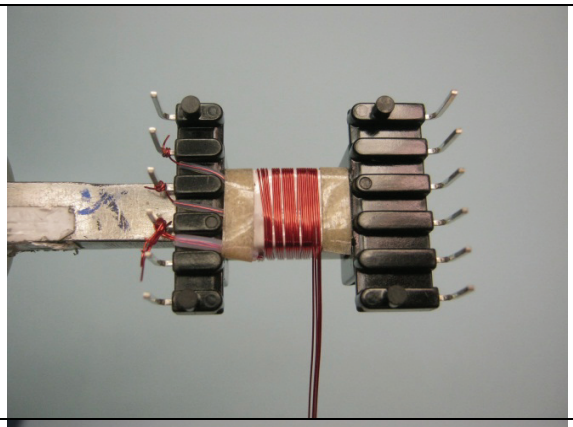
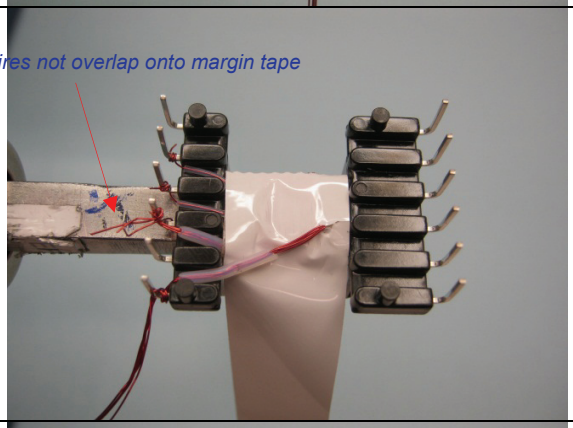
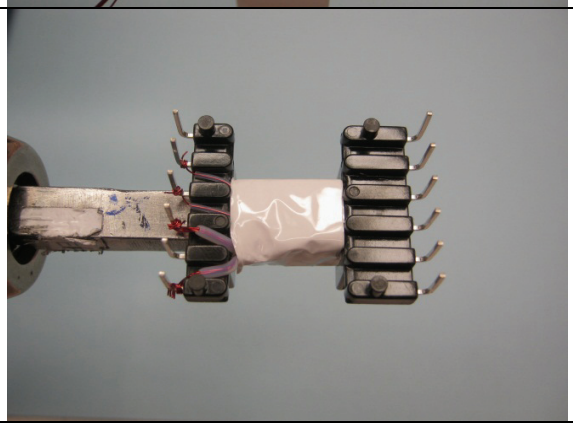
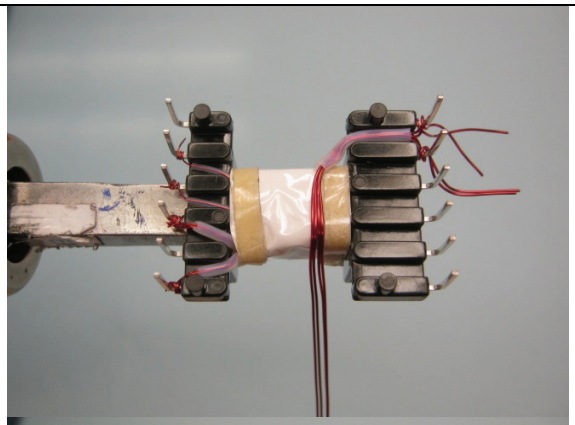
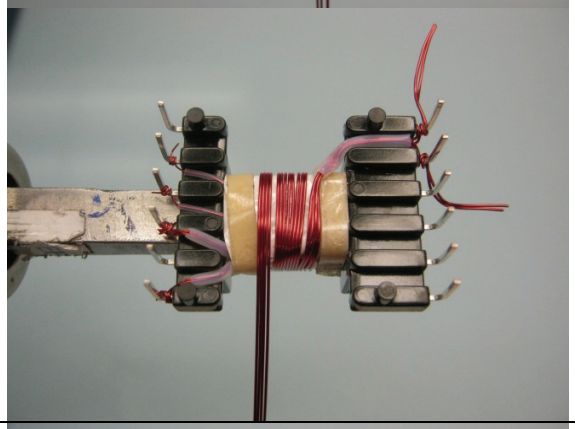
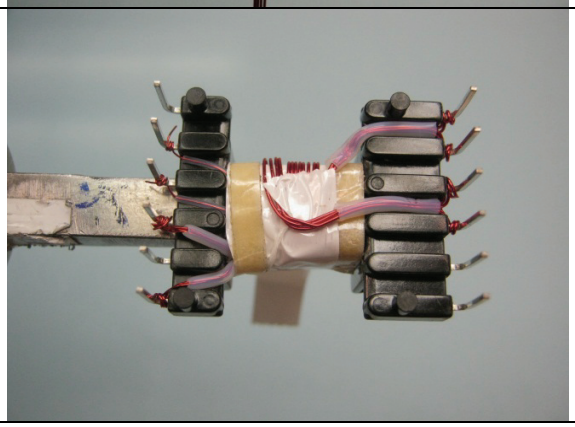
		
		At the last turn bring the wire back to the left, and terminate at pin 1.
Insulation		Place 3 layers of tape item [9].

WD3 **1st Secondary**		 	Start at pins 8, 7, wind 3 quad-filar turns of wire item [4] from right to left, spread the wire evenly,
			At the last turn bring the wire back to the right, and terminate at pin 10, 9.

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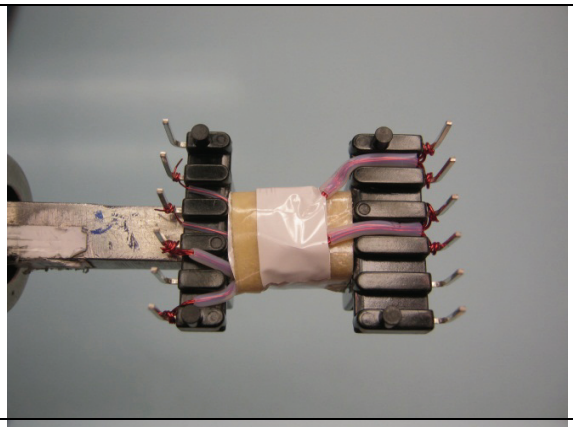
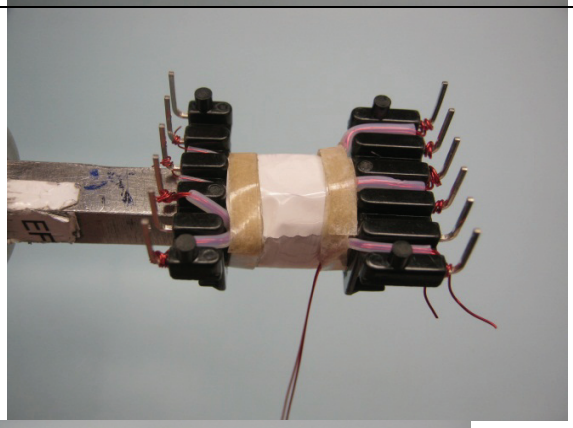
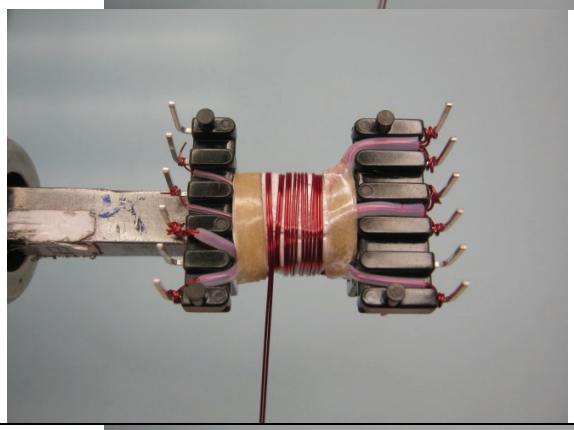
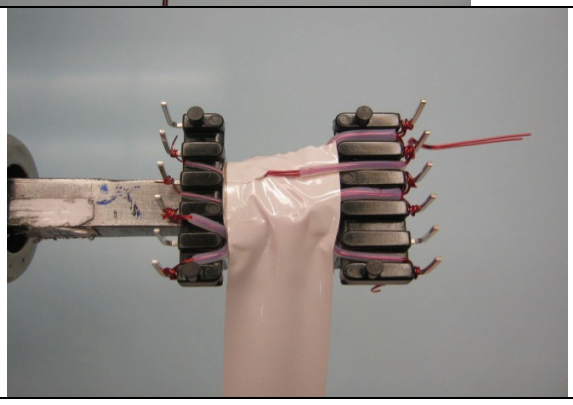
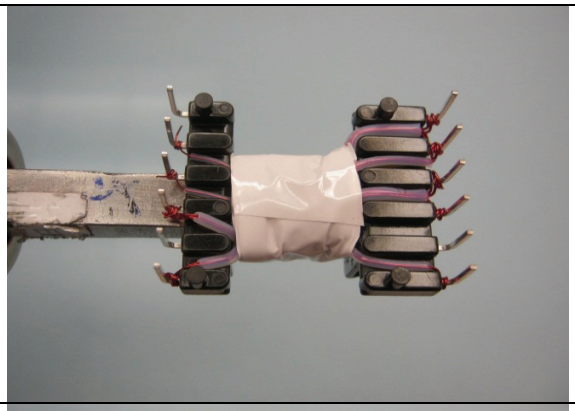
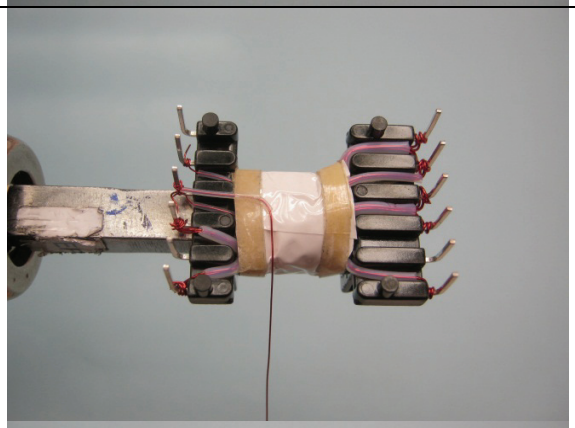
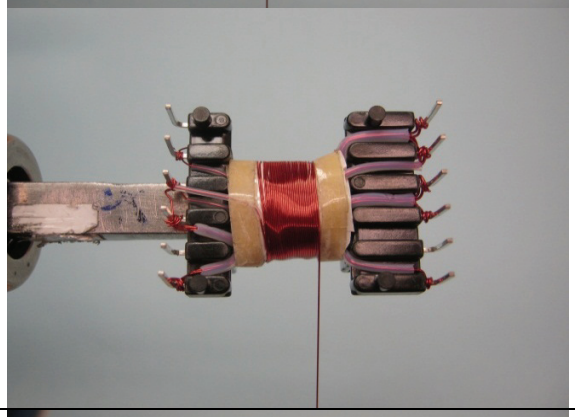
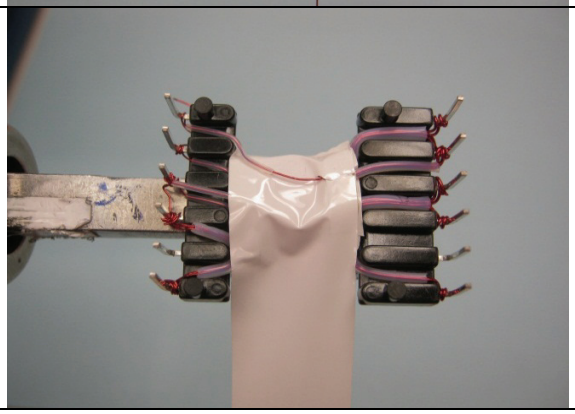
Insulation		Place 1 layer of tape item [8].
WD4 **2nd Secondary**	 	Start at pins 12, wind 7 bi-filar turns of wire item [5] from right to left, spread the wire evenly,
		At the last turn bring the wire back to the right, and terminate at pin 8.

Insulation			Place 3 layers of tape item [9].
WD5 2nd Half Primary		 	Start at pin 4, wind 30 turns of wire item [3] from left to right with tight tension,
			At the last turn bring the wire back to the left, and terminate at pin 6.

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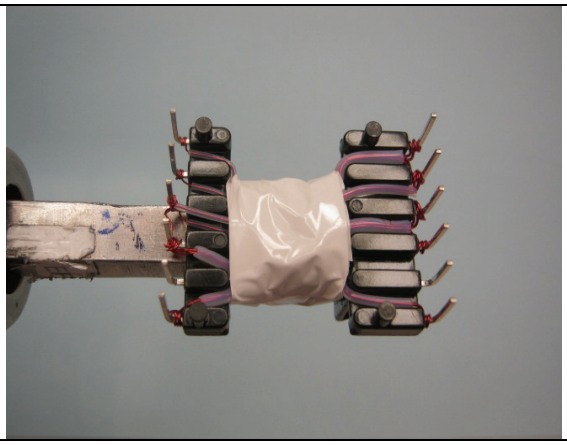
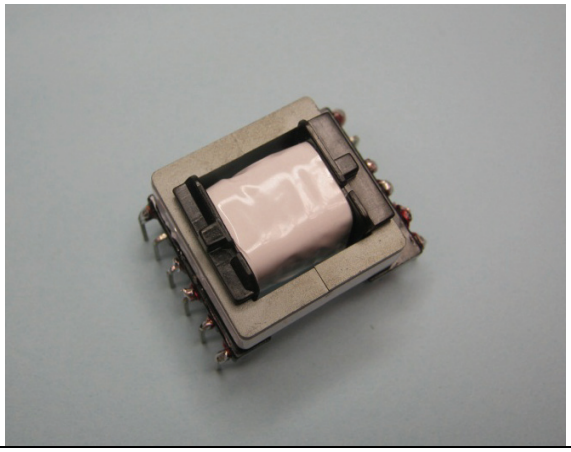
		
Core Assembly		Grind and secure core halves with tape.
Varnish Transformer and Finish		Varnish item [10].

9 性能数据

All measurements performed at room temperature and 50 Hz line frequency, except where otherwise stated. For all tests, the full load is 1000 mA for the 5 V output and 670 mA for the 18 V output (17 W total output power).

9.1 带载模式效率

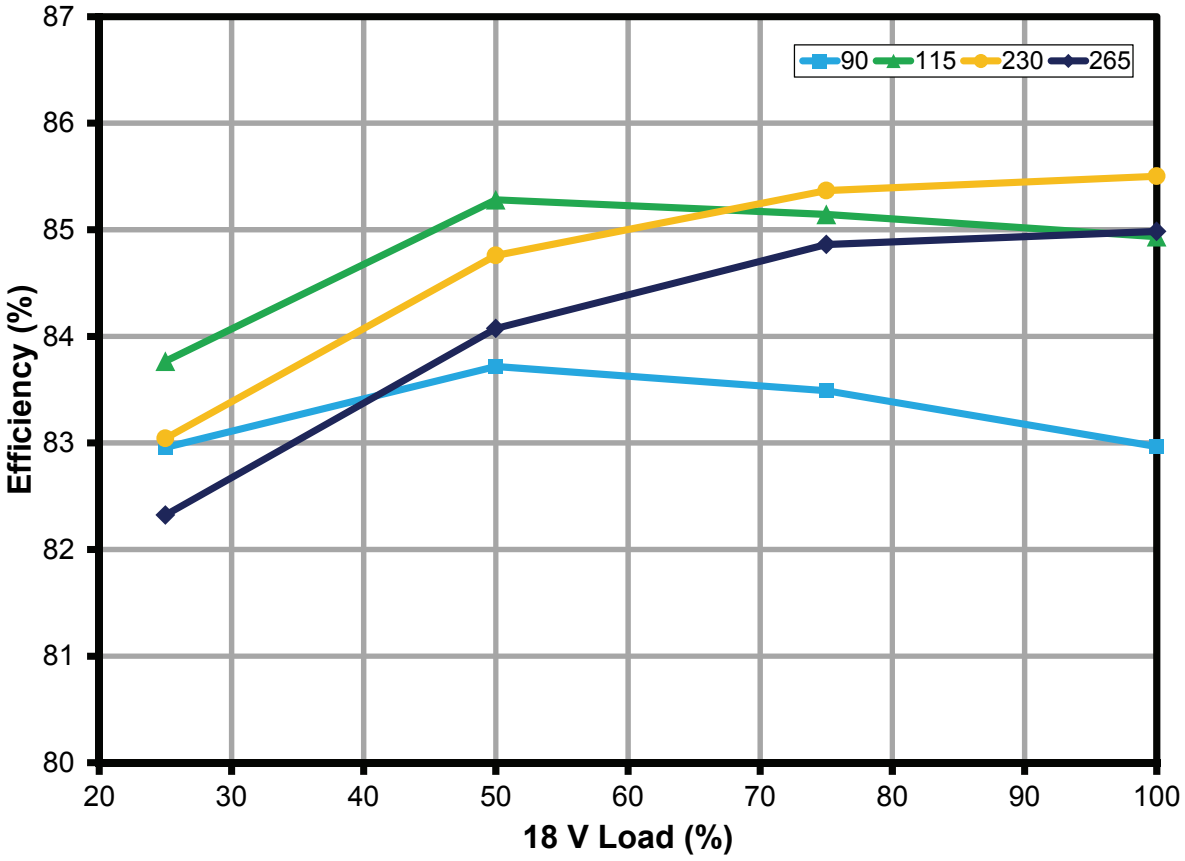


Figure 9 – Efficiency vs. LCD brightness, Room Temperature.

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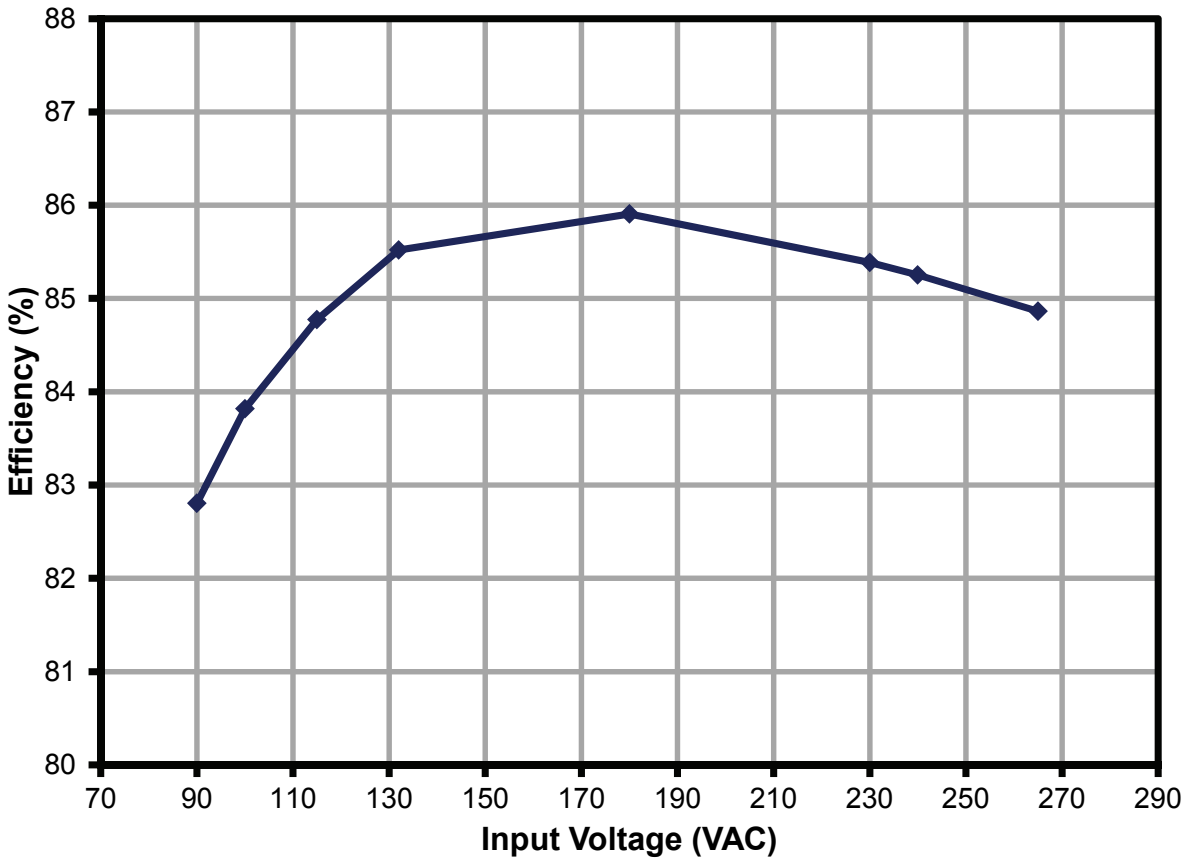

Figure 10 – Full Load Efficiency vs. Input Voltage, Room Temperature.

9.2 待机模式输入功率及待机效率

Standby power and efficiency is measured using a 10 mA load on the 5 V output. The 18 V output is unloaded.

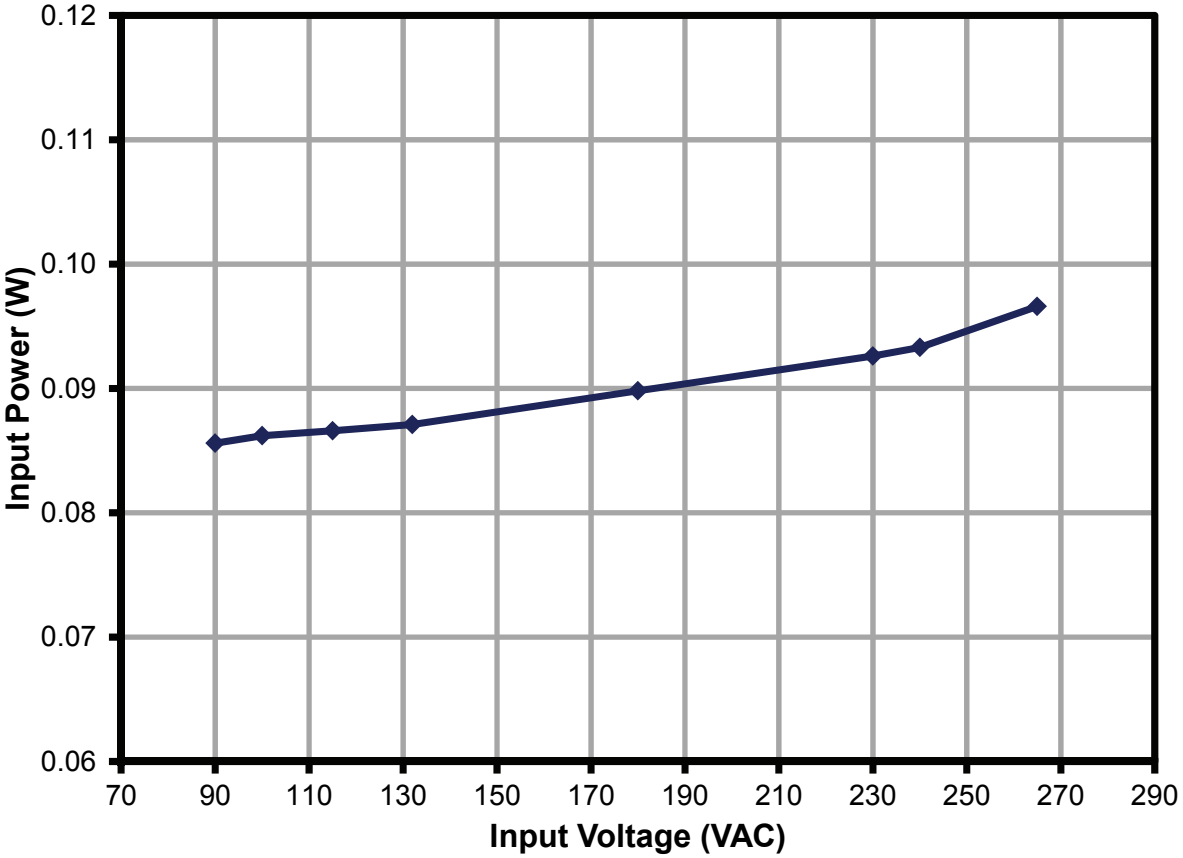

Figure 11 – Standby Input Power vs. Input Line Voltage, Room Temperature.

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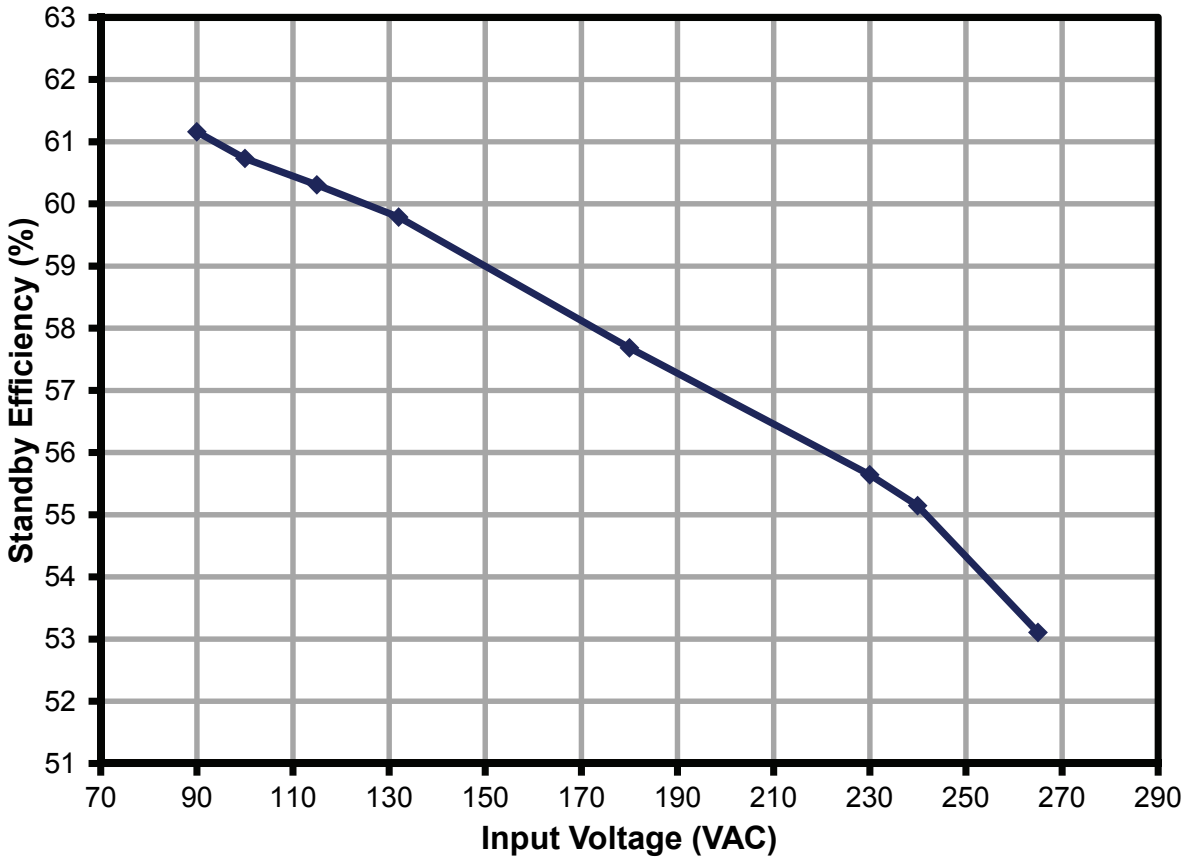

Figure 12 – Standby Efficiency vs. Input Voltage, Room Temperature.

9.3 18 V 0.67 A DC负载和5 V 1 A平均负载下的线电压调整

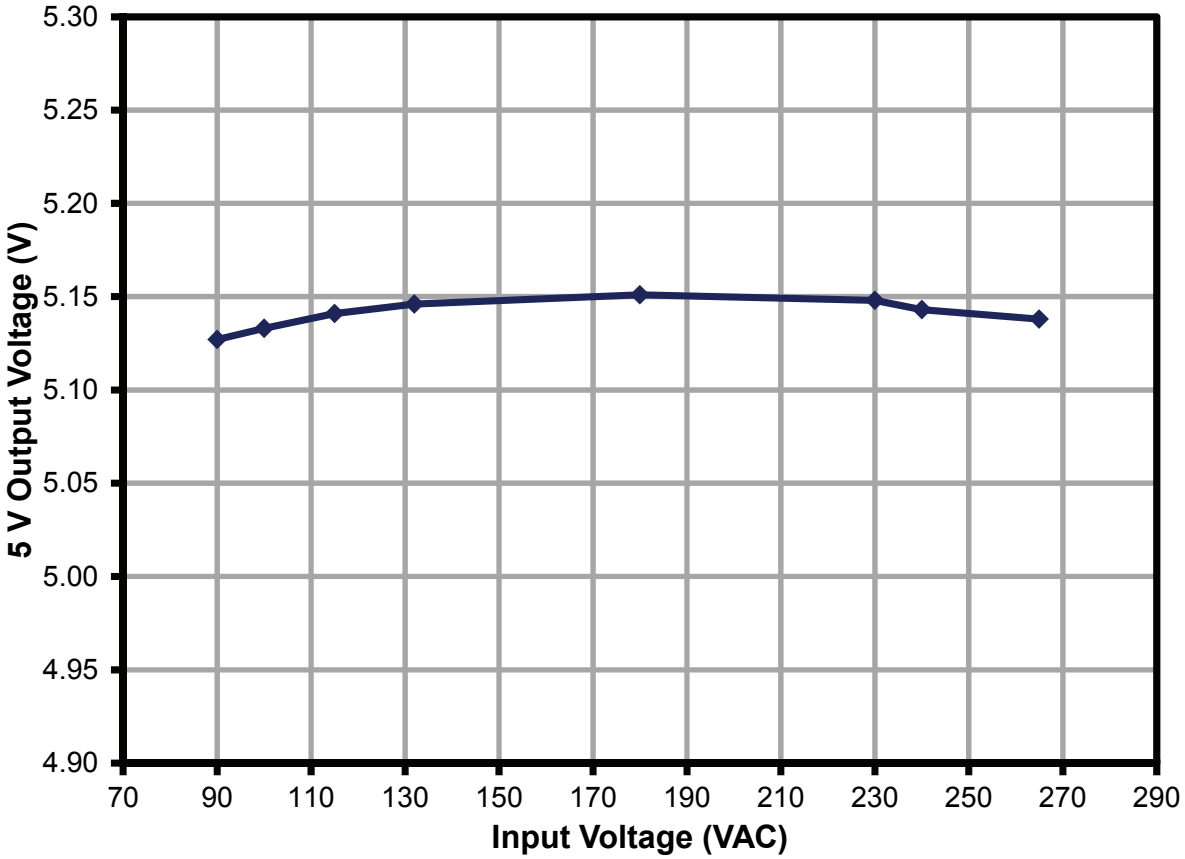

Figure 13 – 5 V Line Regulation under Full Load.

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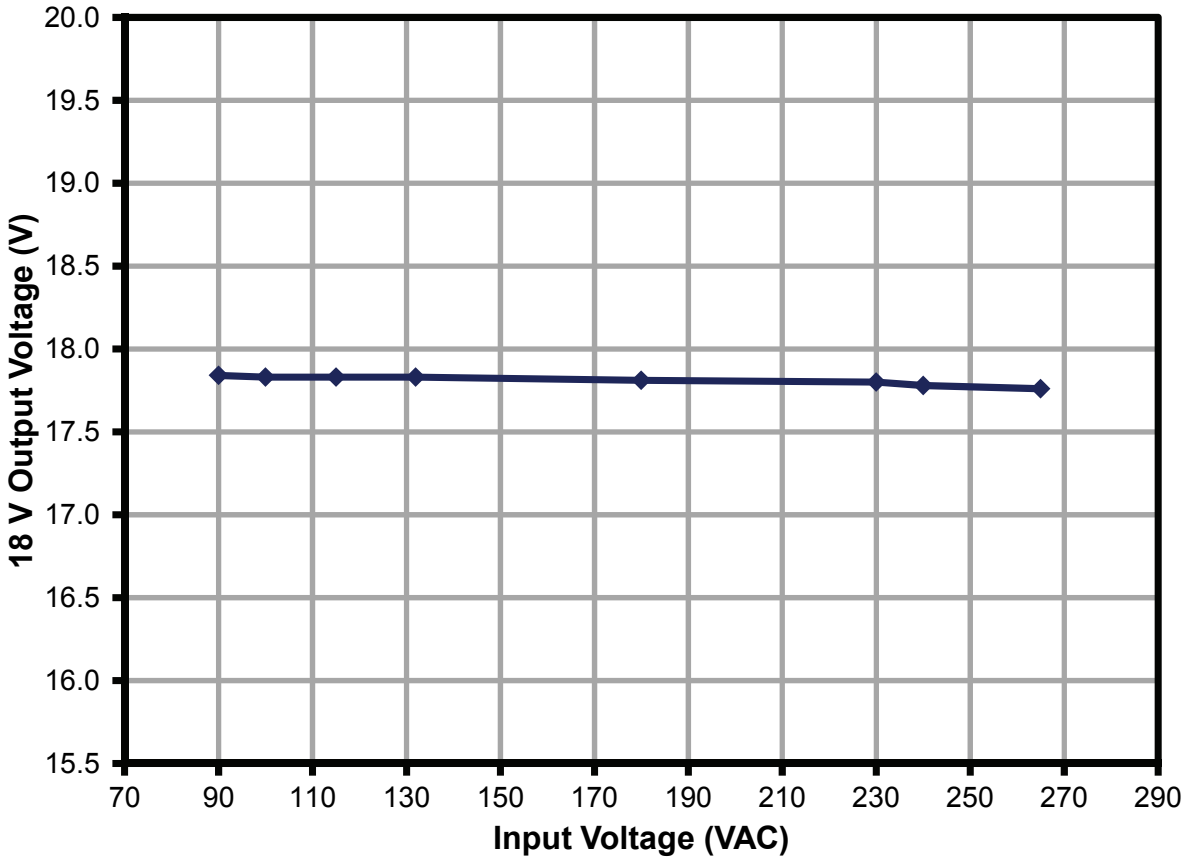

Figure 14 – 18 V Line Regulation under Full Load.

9.4 指定动态负载间档下的输出电压（包括峰值、最小值和平均值）

9.4.1 峰值和最小输出电压的测试方法

Figure 15 shows how the peak value and minimum value were collected. The power supply was loaded with the specified load profile in Figure 3. 18 V output load (LCD brightness) is always a pulsed load from 0 to 0.67 A with different duty cycle and 5 V load is always transient from 0.5 A to 1.5 A. Scope were used to record the peak value and minimum value for both output voltage, and the mean value is recorded with multimeter.

Figure 15 – Test Method for Peak and Minimum Output Voltage.

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9.4.2 指定负载间档下的5 V输出电压

Figures below shows mean regulation (measured with multimeter), peak and minimum output voltage (measured with scope) under specified dynamic load profile.

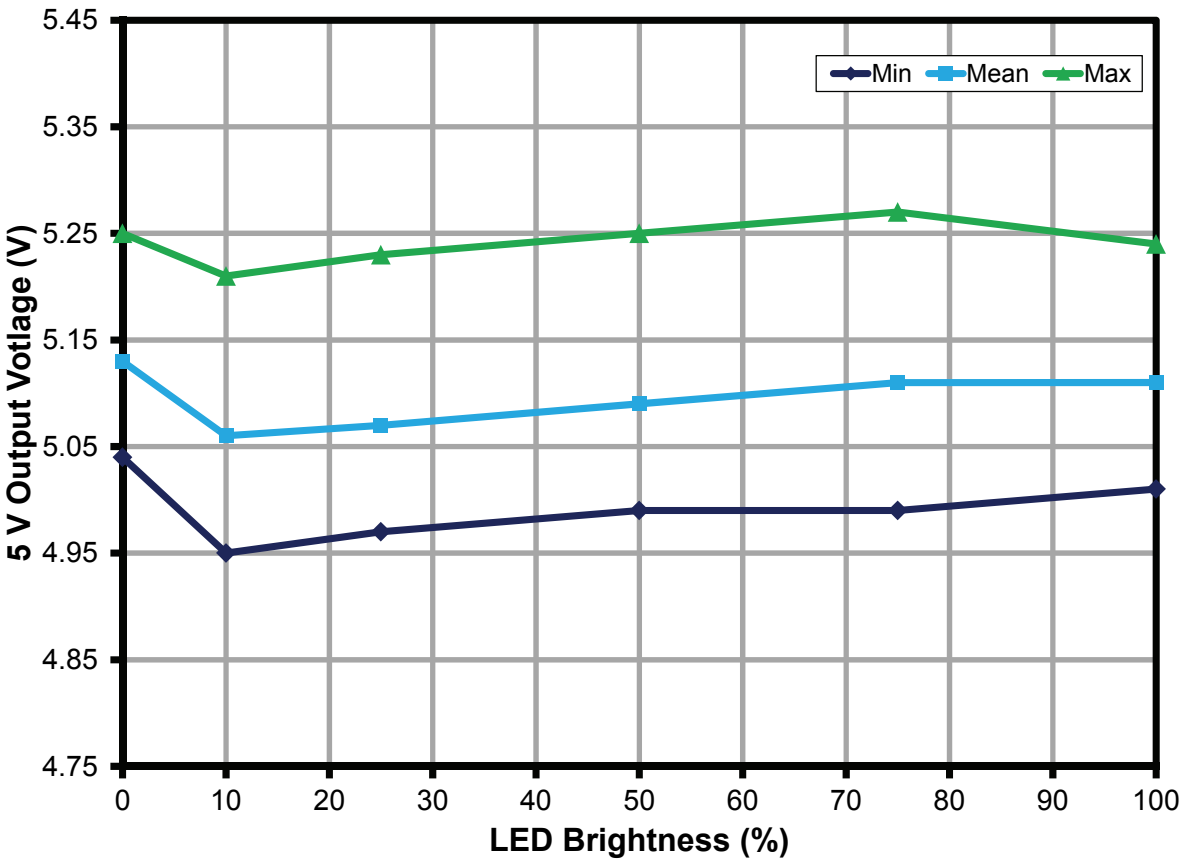

Figure 16 – 5 V Output Voltage under Specified Load Profile at 90 VAC.

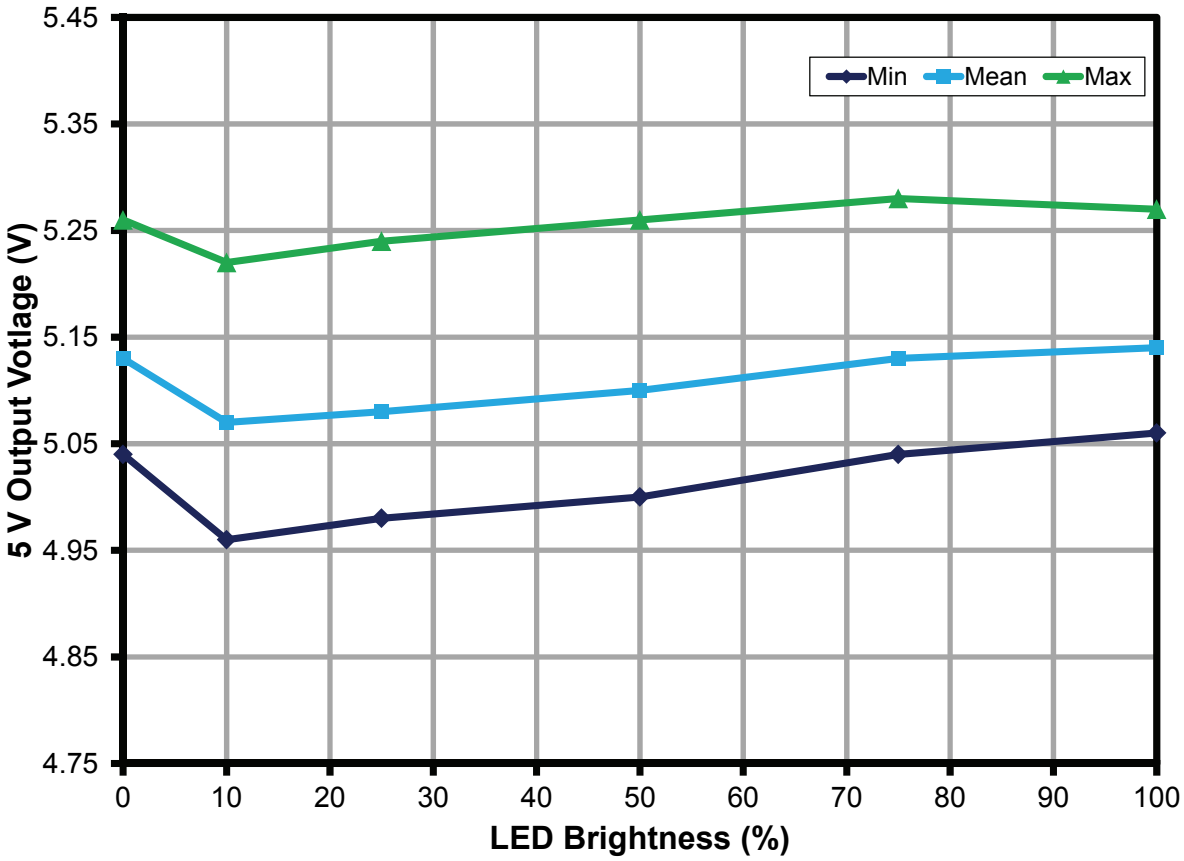

Figure 17 – 5 V Output Voltage under Specified Load Profile at 115 VAC.

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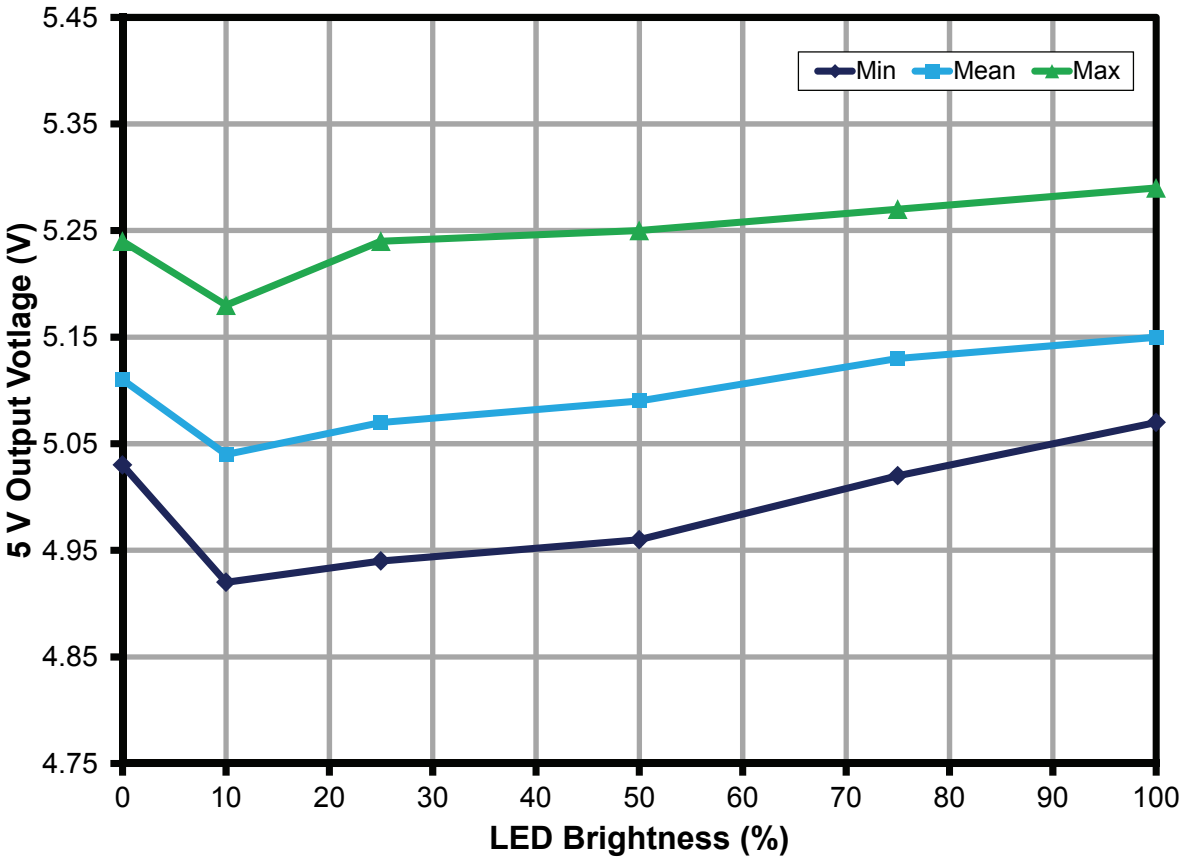

Figure 18 – 5 V Output Voltage under Specified Load Profile at 230 VAC.

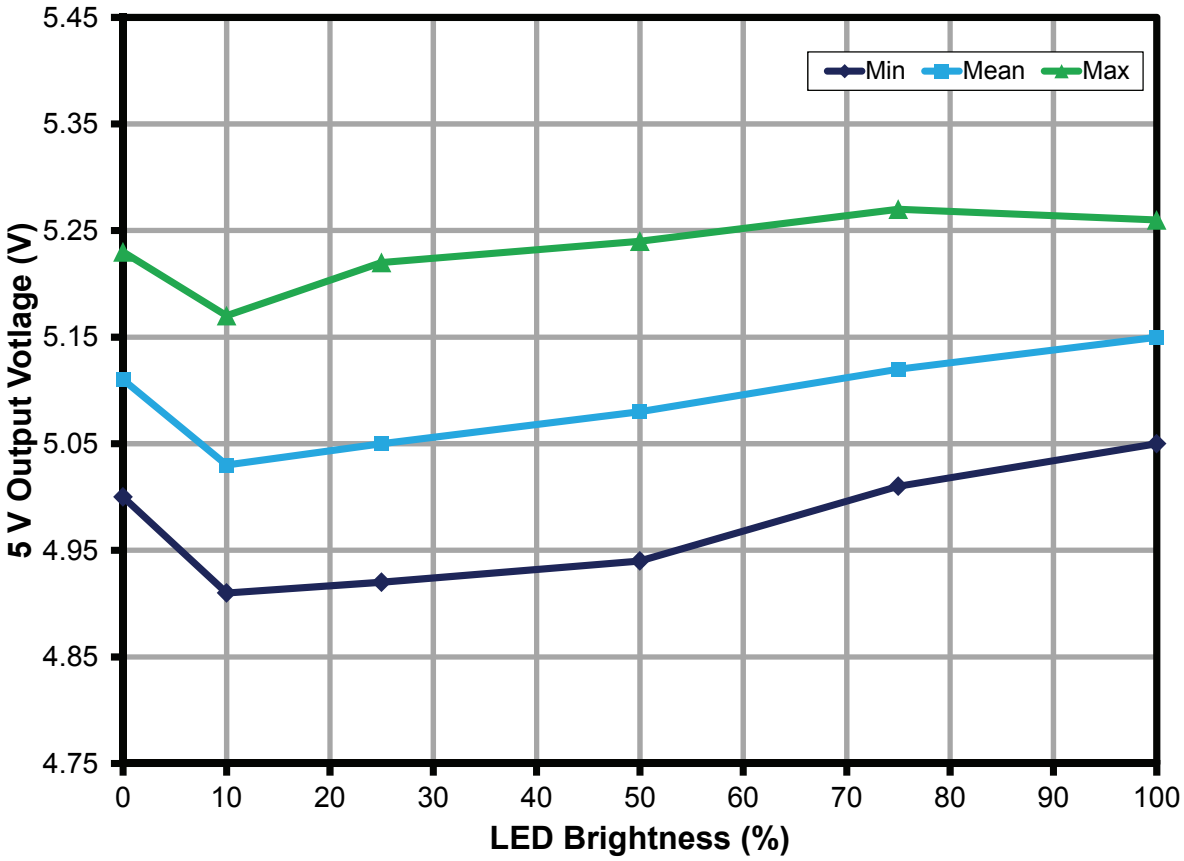

Figure 19 – 5 V Output Voltage under Specified Load Profile at 265 VAC.

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9.4.3 指定负载间档下的18 V输出电压

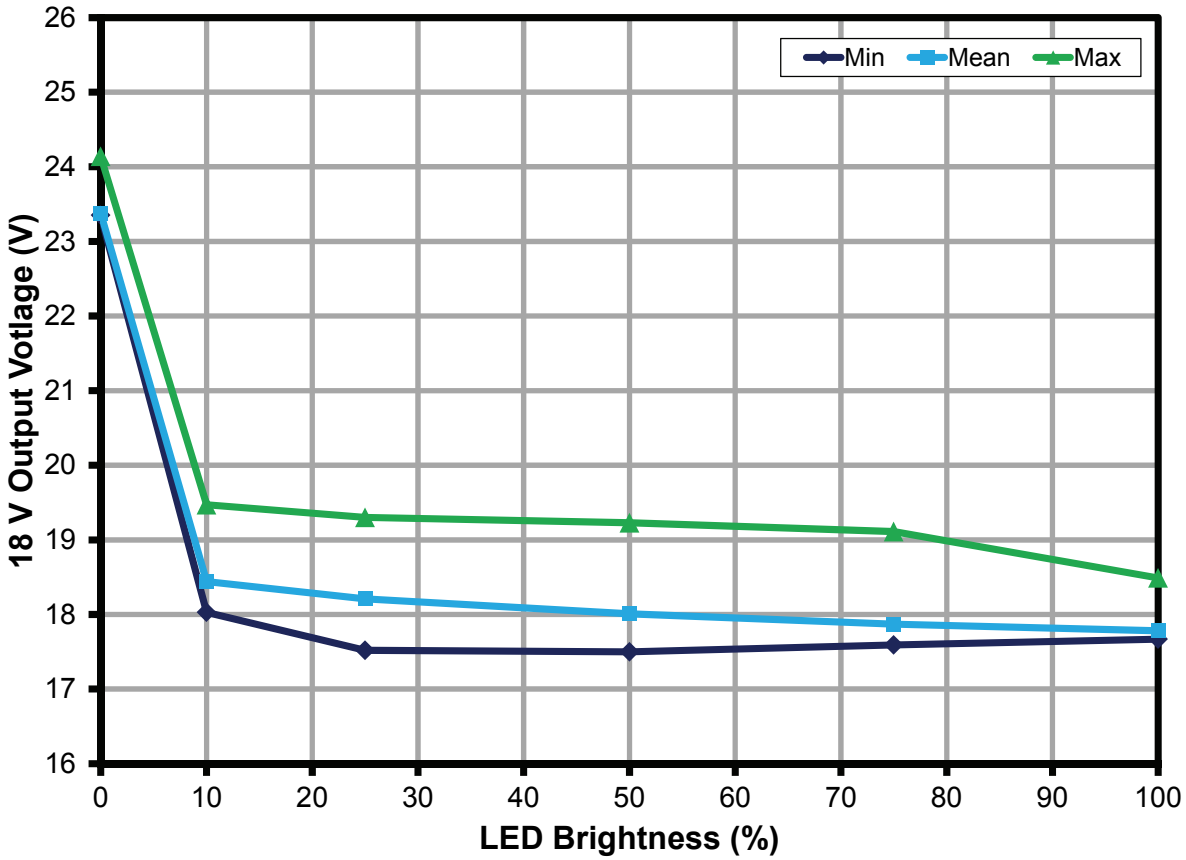

Figure 20 – 18 V Output Voltage under Specified Load Profile at 90 VAC

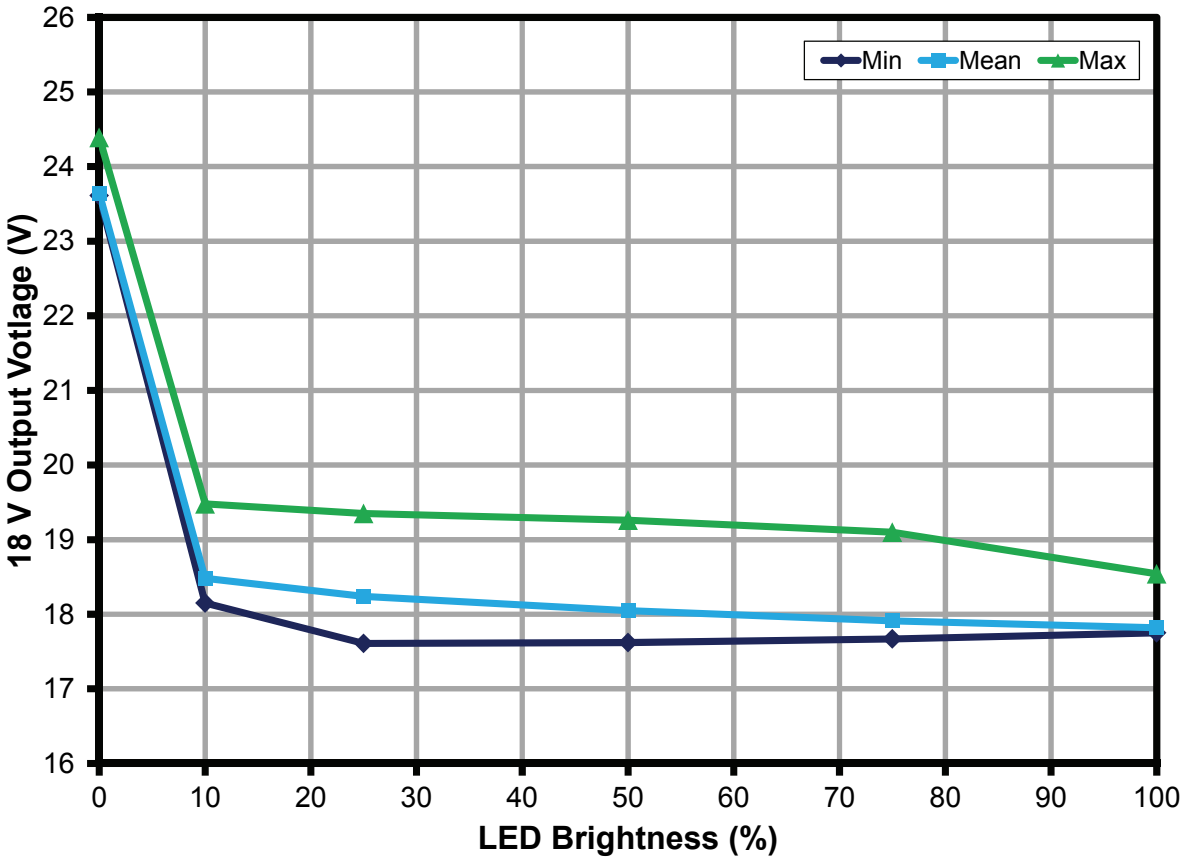

Figure 21 – 18 V Output Voltage under Specified Load Profile at 115 VAC.

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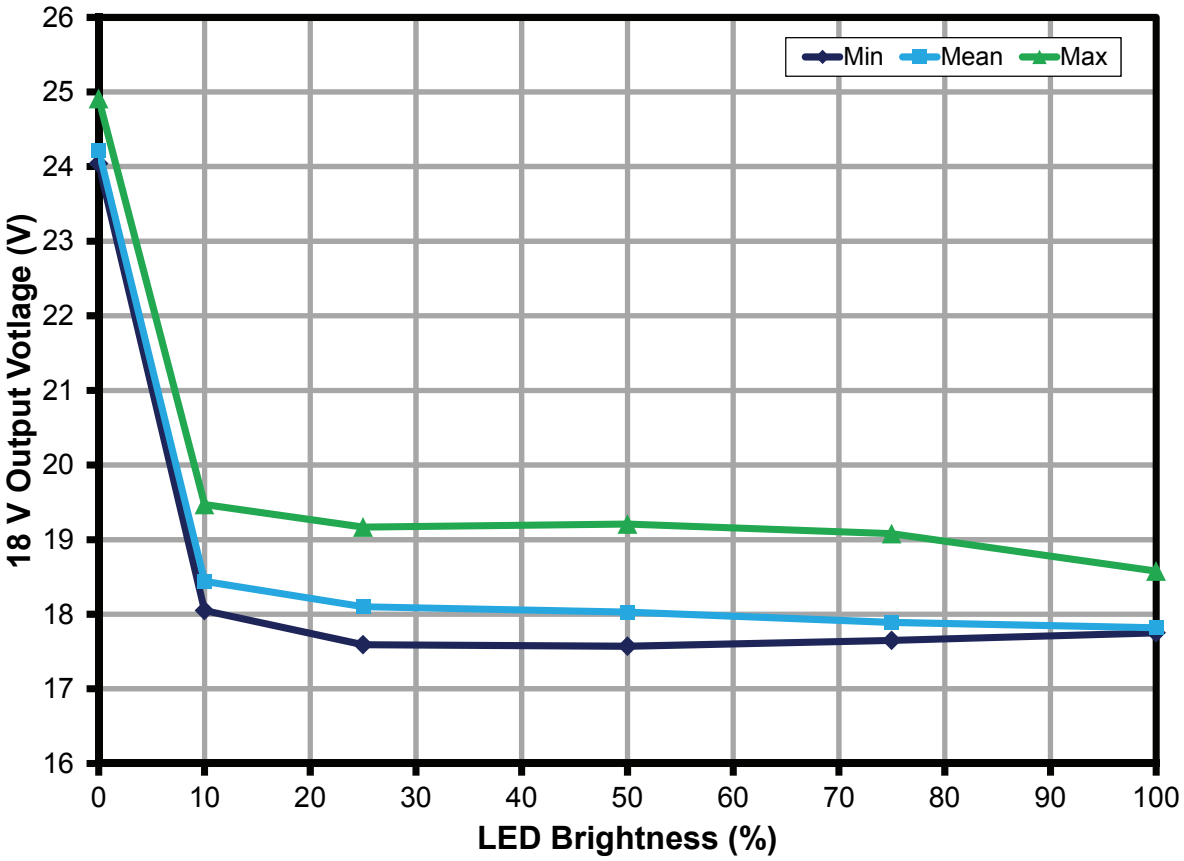

Figure 22 – 18 V Output Voltage under Specified Load Profile at 230 VAC.

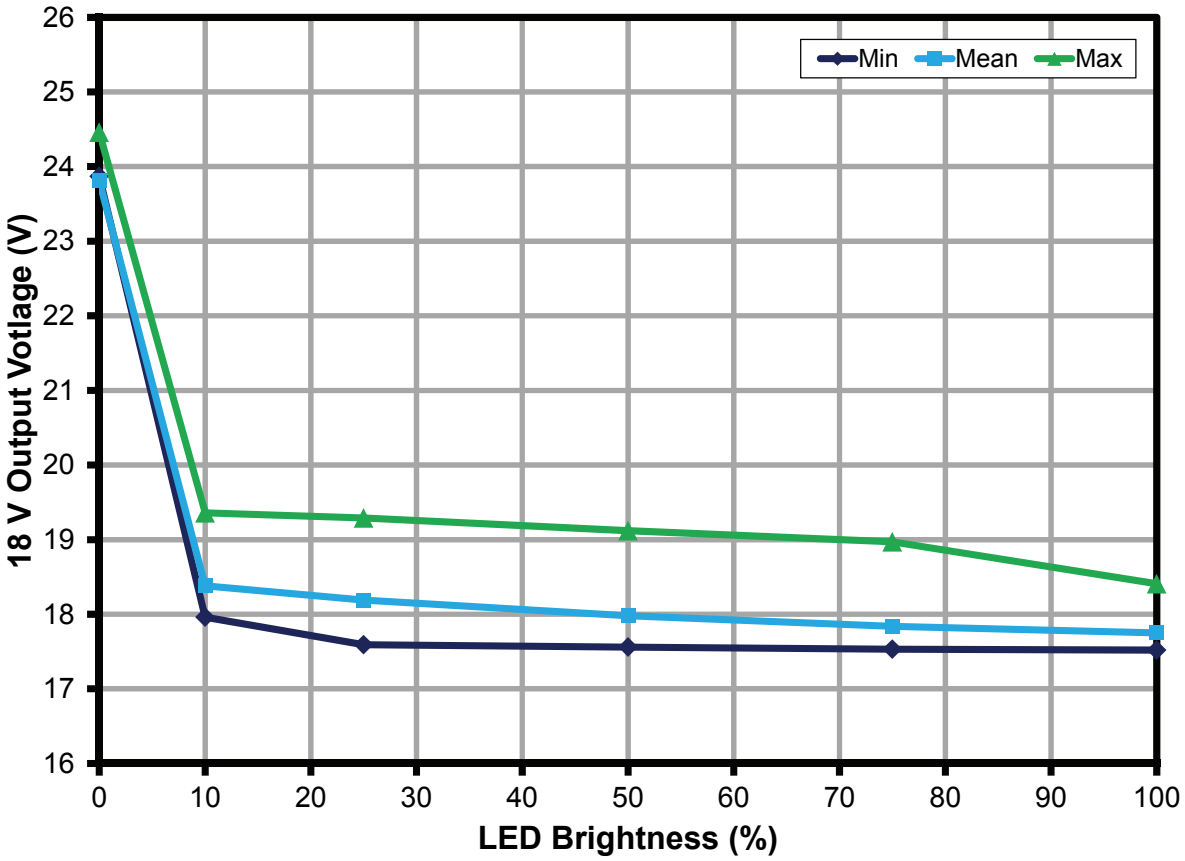

Figure 23 – 18 Output Voltage under Specified Load Profile at 265 VAC.

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10 热性能

The unit was allowed to reach thermal equilibrium prior to the measurement. Figure 24 is the temperature profile of the board at room temperature.

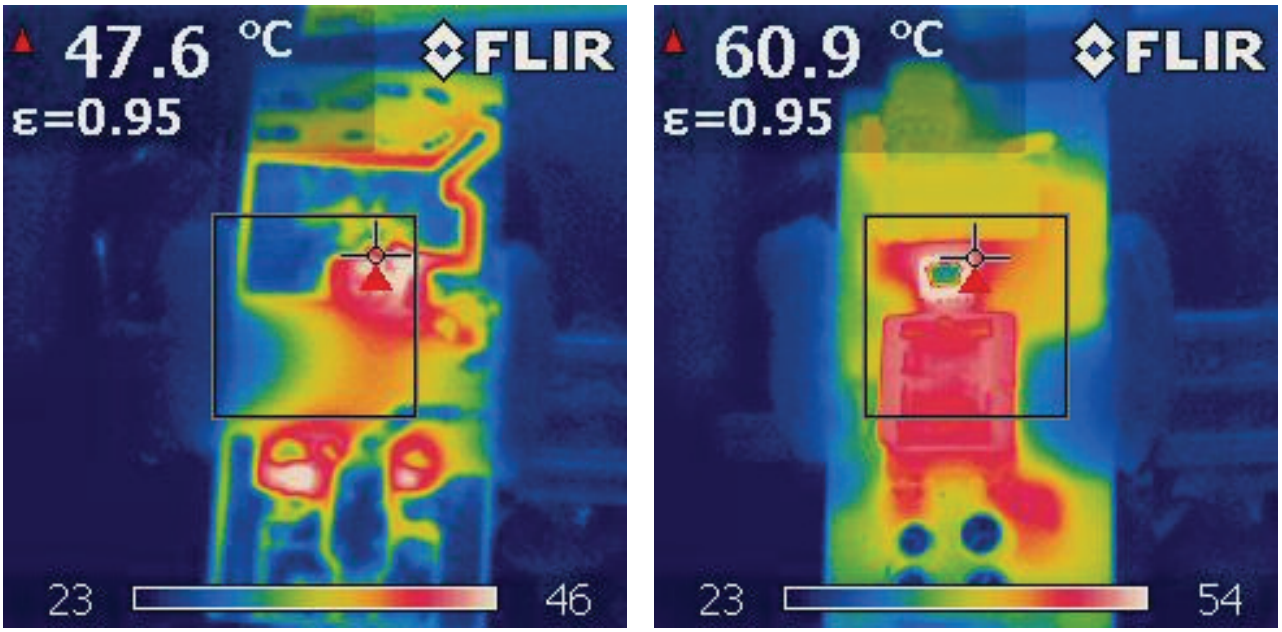

Figure 24 – Top (Right) and Bottom (left) Side Thermal Images at 265 VAC, Full Load, Room Temperature.

Table below shows the temperature of key components at 40 °C .The power supply was sealed into a box first, and the box was placed into a thermal chamber with 40 °C ambient. Temperatures of LinkSwitch-HP SOURCE pin and cathode pin of the output diode were measured at system full load (18 V/0.67 A, 5 V/1 A average). Temperature was recorded after the thermal reading was stable.

Temperature measurements of key components were taken using T-type (Copper-Constantan) thermocouples. The thermocouples were soldered directly to a SOURCE pin of the LNK6774V device and to the cathode of the output rectifier. The thermocouples were glued to the external core and to winding surfaces of the transformer.

The unit was sealed inside a large box to eliminate any air currents. The ambient temperature outside the box was raised to 40 °C. The unit was then operated at full load (5 V, 1 A and 18 V 0.67 A) and the temperature measurements were taken after they stabilized for 1 hour at 40 °C.

Temperature (°C)		
Item	**90 VAC**	**265 VAC**
LN6774V (U1)	76	79
5 V Output Diode	63	63
18 V Output Diode	61	61
Transformer	61	68

These results show that the IC has an acceptable rise in temperature.

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11 波形

11.1 漏极电压和电流，正常工作

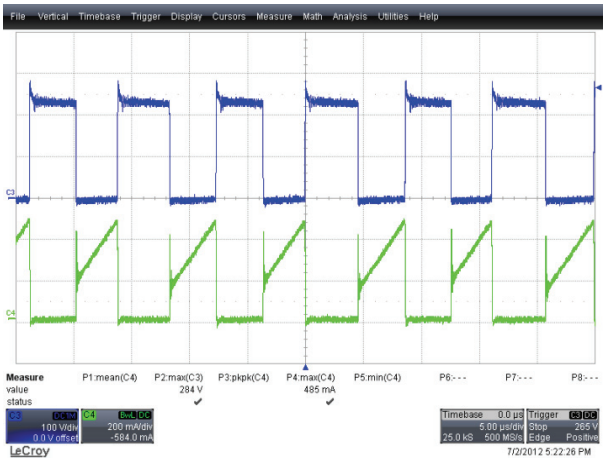

Figure 25 – 90 VAC, Full Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.2 A, 5 µs / div.

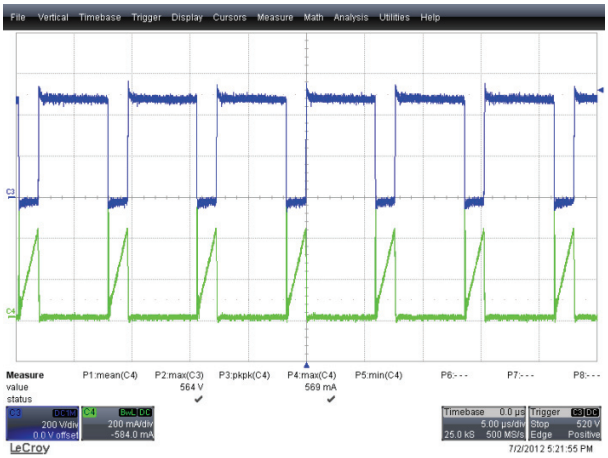

Figure 26 – 265 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.2 A, 5 µs / div.

11.2 漏极电压和电流启动特征

Drain and current profile during startup was tested with 5 V average 1 A load and 18 V no-load, since the power supply always start up into 18 V no load based on the specification. 5 V was tested with the dynamic load specified in the specification.

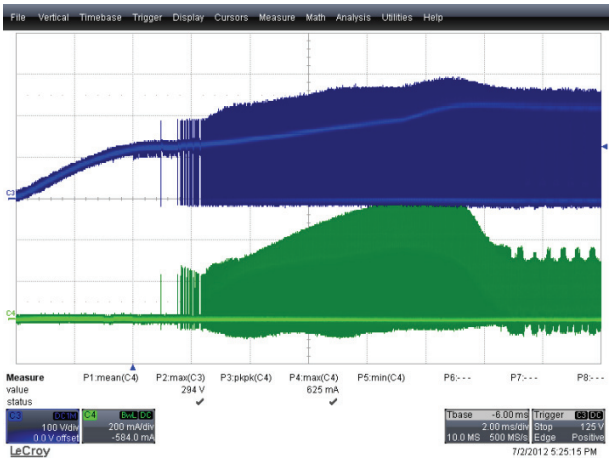

Figure 27 – 90 VAC, 5 V Dynamic, 18 V No-Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.2 A, 2 ms / div.

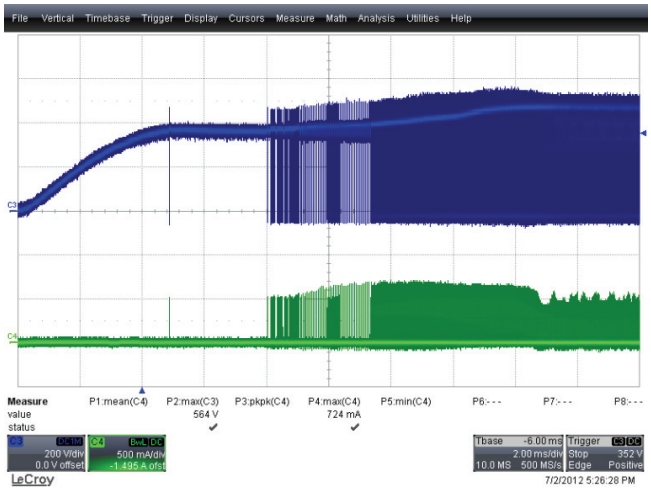

Figure 28 – 265 VAC 5 V Dynamic, 18 V No-Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.5 A, 2 ms / div.

11.3 输出电压启动特征（相对于输入电压）

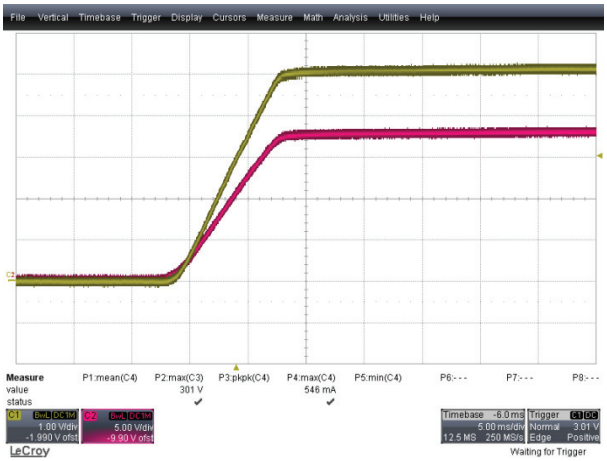

Figure 29 – Start-up Profile, 90 VAC, Standby Load.
Upper: V_{OUT}, 5 V, 1 V / div.
Lower: V_{OUT}, 18 V, 5 V, 5 ms / div.

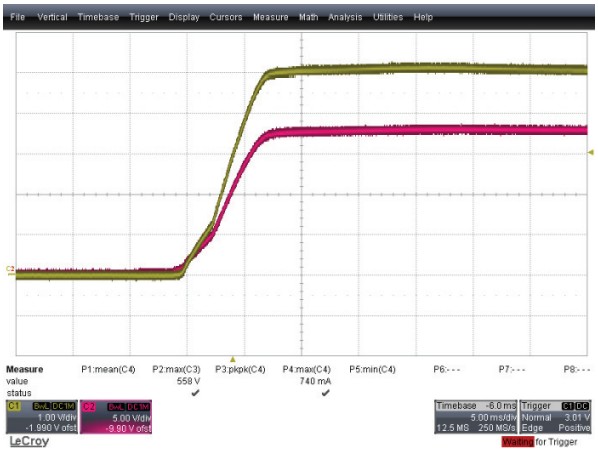

Figure 30 – Start-up Profile, 265 VAC, Standby Load.
Upper: V_{OUT}, 5 V, 1 V / div.
Lower: V_{OUT}, 18 V, 5 V, 5 ms / div.

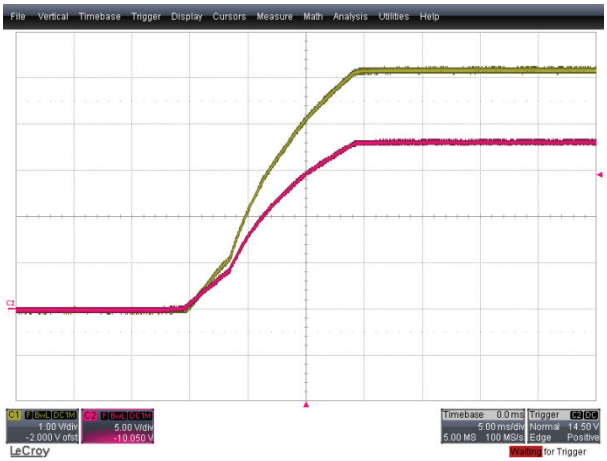

Figure 31 – Start-up Profile, 90 VAC, Full CC Load.
Upper: V_{OUT}, 5 V, 1 V / div.
Lower: V_{OUT}, 18 V, 5 V, 5 ms / div.

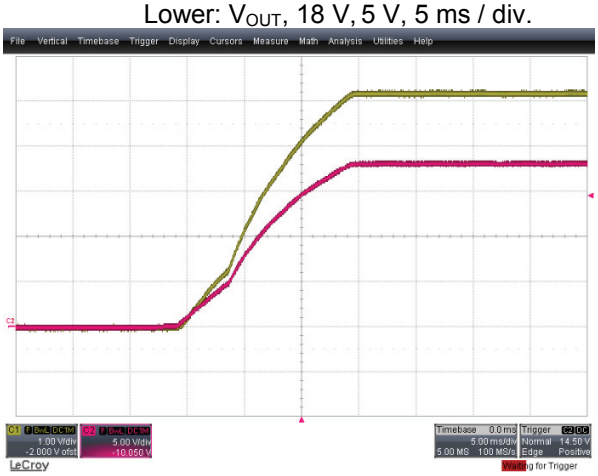

Figure 32 – Start-up Profile, 265 VAC, Full CC Load.
Upper: V_{OUT}, 5 V, 1 V / div.
Lower: V_{OUT}, 18 V, 5 V, 5 ms / div.

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11.4 5 V负载瞬态响应

11.4.1 采用5 V、500 mA至1500 mA阶跃负载和固定的18 V, 0.67 A DC负载进行5 V瞬态测试

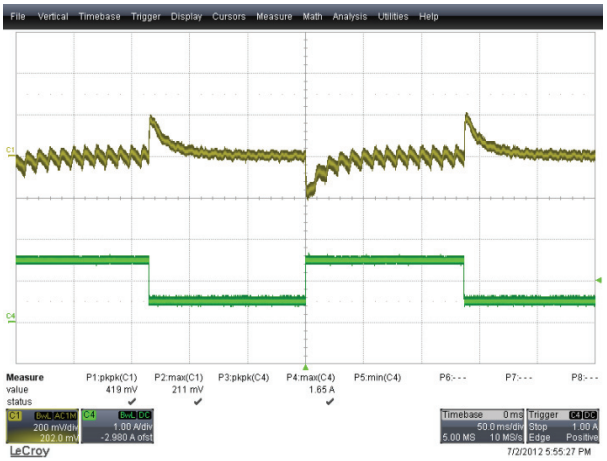

Figure 33 – 90 VAC, 18 V 0.67 A.
Upper: V_{OUT}, 5 V, 200 mV / div.
Lower: I_{OUT}, 5 V, 1 A, 50 ms / div.

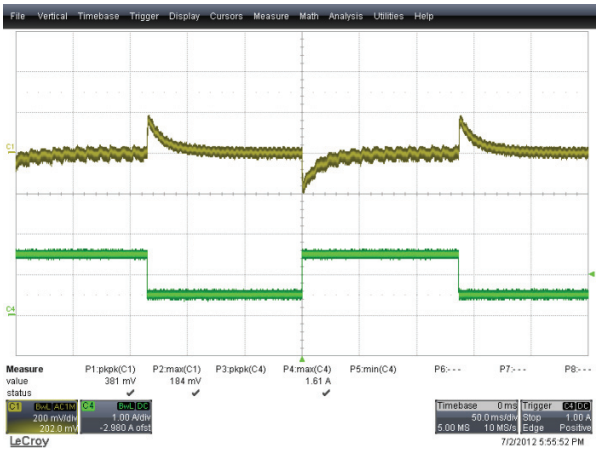

Figure 34 – 115 VAC, 18 V 0.67 A.
Upper: $V_{OUT,}$ 5 V, 200 mV / div.
Lower: I_{OUT}, 5 V, 1 A, 50 ms / div.

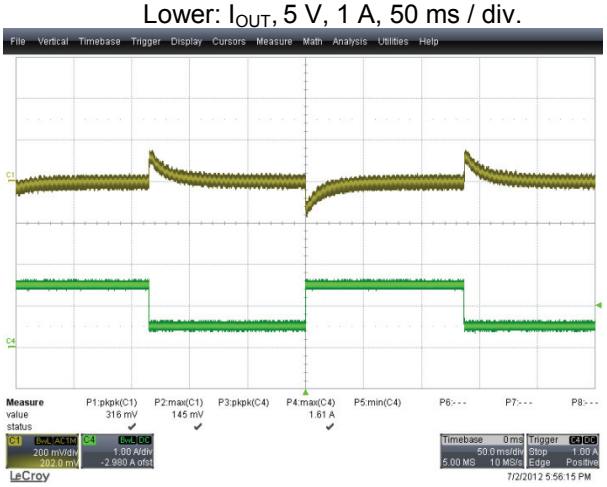

Figure 35 – 230 VAC, 18 V 0.67 A.
Upper: V_{OUT}, 5 V, 200 mV / div.
Lower: I_{OUT}, 5 V, 1 A, 50 ms / div.

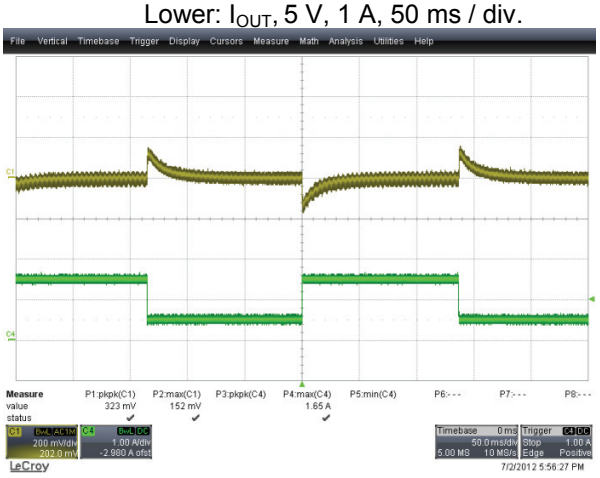

Figure 36 – 265 VAC, 18 V 0.67 A.
Upper: V_{OUT}, 5 V, 200 mV / div.
Lower: I_{OUT}, 5 V, 1 A, 50 ms / div.

11.4.2 采用指定负载间档进行5 V瞬态测试

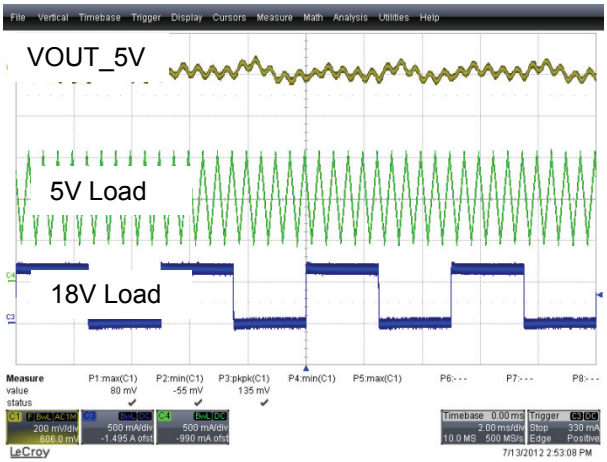

Figure 37 – 90 VAC, 5 V 1 A Dynamic Load and 18 V 0 to 0.67 A Step Load.
Upper: V_{OUT}, 5 V, 100 mV / div.
Lower: I_{OUT}, 18 V, 0.5 A, 5 ms / div.

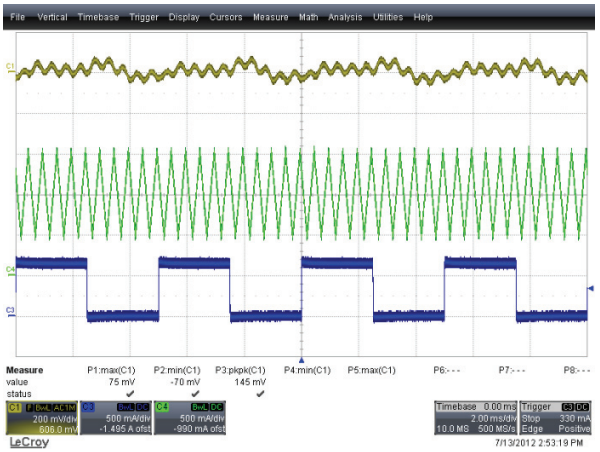

Figure 38 – 115 VAC, 5 V 1 A Dynamic Load and 18 V 0 to 0.67 A Step Load.
Upper: $V_{OUT,}$ 5 V, 100 mV / div.
Lower: $I_{OUT,}$ 18 V, 0.5 A, 5 ms / div.

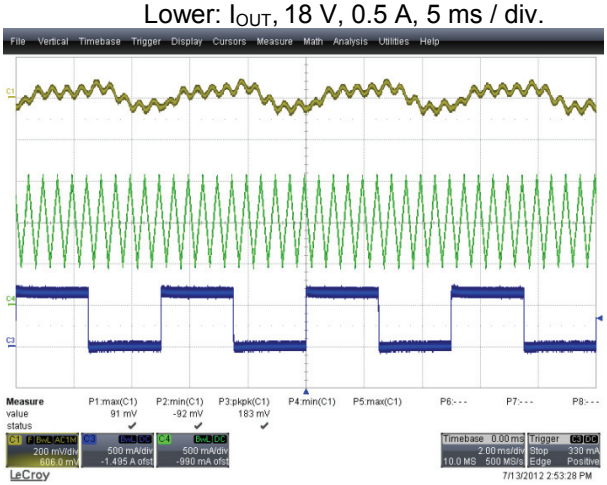

Figure 39 – 230 VAC, 5 V 1 A Dynamic Load and 18 V 0 to 0.67 A Step Load.
Upper: V_{OUT}, 5 V, 100 mV / div.
Lower: I_{OUT}, 18 V, 0.5 A, 5 ms / div.

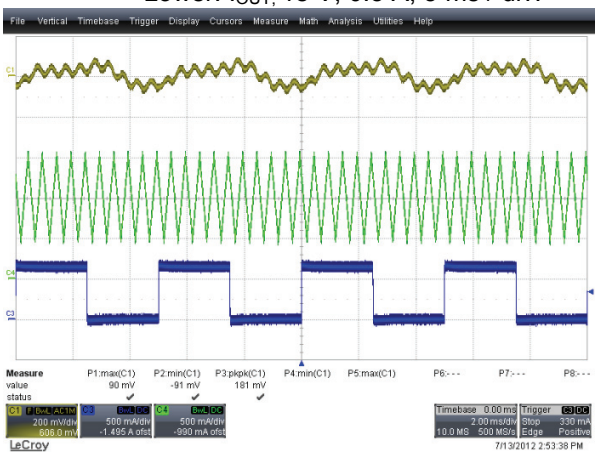

Figure 40 – 265 VAC, 5 V 1 A Dynamic Load and 18 V 0 to 0.6 A Step Load.
Upper: V_{OUT}, 5 V, 100 mV / div.
Lower: I_{OUT}, 18 V, 0.5 A, 5 ms / div.

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11.4.3 采用指定负载间档进行18 V瞬态测试

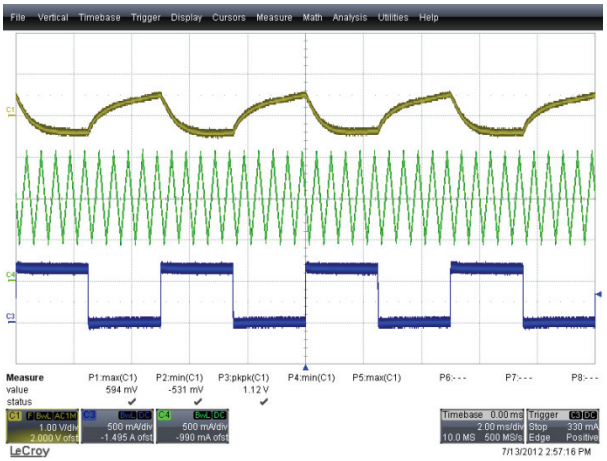

Figure 41 – 90 VAC, 5 V 1 A Average Load.
Upper: V_{OUT}, 18 V, 1 V / div.
Lower: I_{OUT}, 18 V, 0.5 A, 5 ms / div.

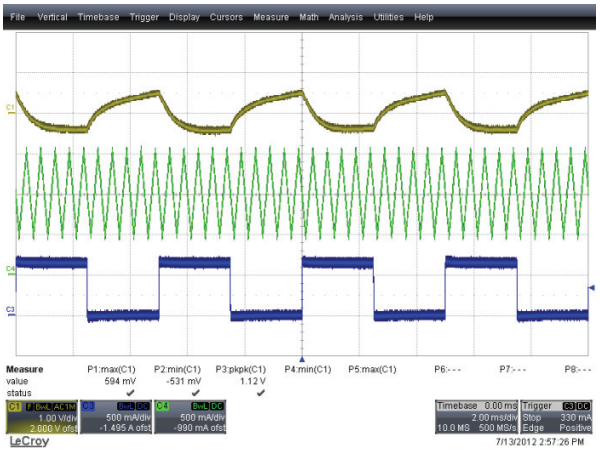

Figure 42 – 115 VAC, 5 V 1 A Average Load.
Upper: V_{OUT}, 18 V, 1 V / div.
Lower: I_{OUT}, 18 V, 0.5 A, 5 ms / div.

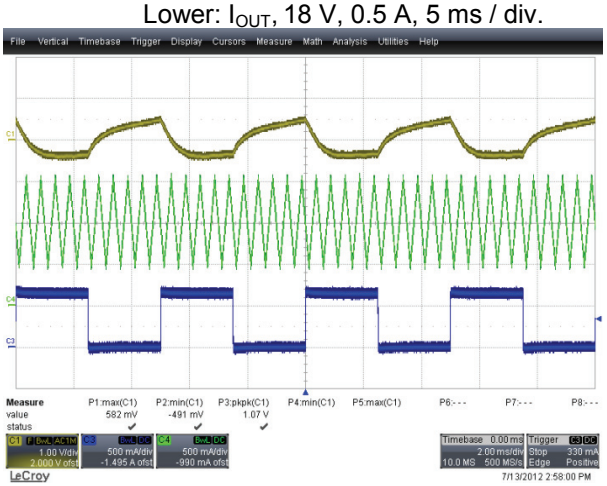

Figure 43 – 230 VAC, 5 V 1 A Average Load.
Upper: V_{OUT}, 18 V, 1 V / div.
Lower: I_{OUT}, 18 V, 0.5 A, 5 ms / div.

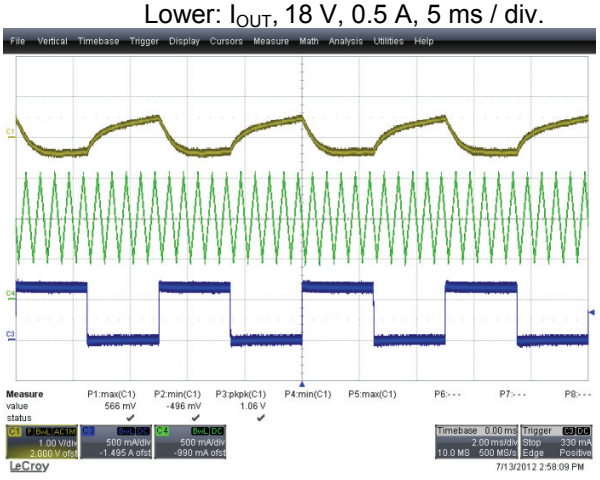

Figure 44 – 265 VAC, 5 V 1 A Average Load.
Upper: V_{OUT}, 18 V, 1 V / div.
Lower: I_{OUT}, 18 V, 0.5 A, 5 ms / div.

11.5 输出纹波和噪声测量

11.5.1 纹波测量技巧

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the figures below.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 1.0 μF / 50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

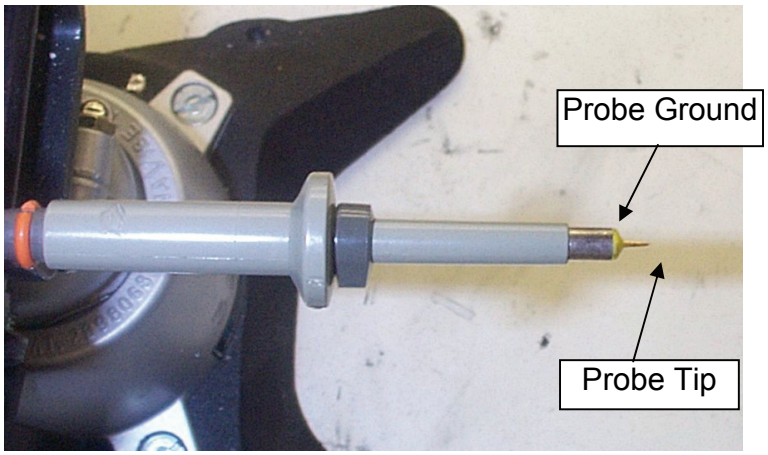

Figure 45 – Oscilloscope Probe Prepared for Ripple Measurement.
(End Cap and Ground Lead Removed).

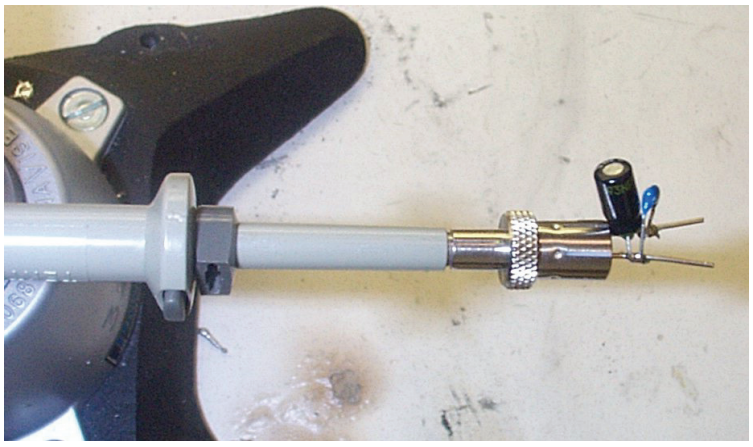

Figure 46 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added).

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11.5.2 在18 V最大负载和5 V 1 A稳态负载下测试18 V纹波

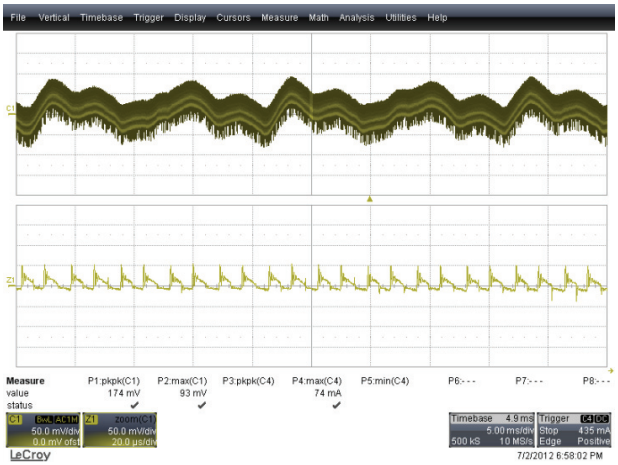

Figure 47 – 18 V Ripple, 90 VAC, Full Load.
Upper: 18 V_{RIPPLE}, 5 ms, 50 mV / div.
Lower: 18 V_{RIPPLE}, 20 µs, 50 mV / div.

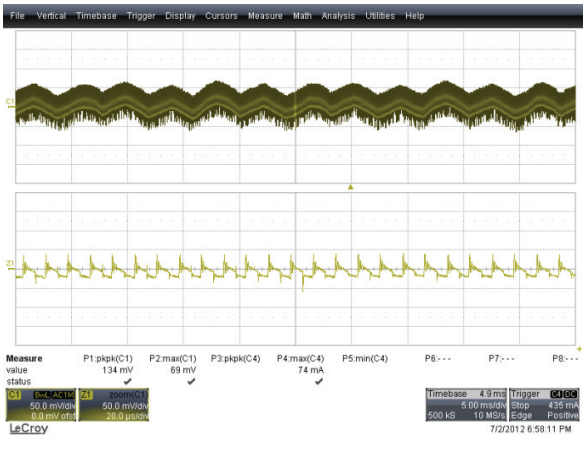

Figure 48 – 18 V Ripple, 115 VAC, Full Load.
Upper: 18 V_{RIPPLE}, 5 ms, 50 mV / div.
Lower: 18 V_{RIPPLE}, 20 µs, 50 mV / div.

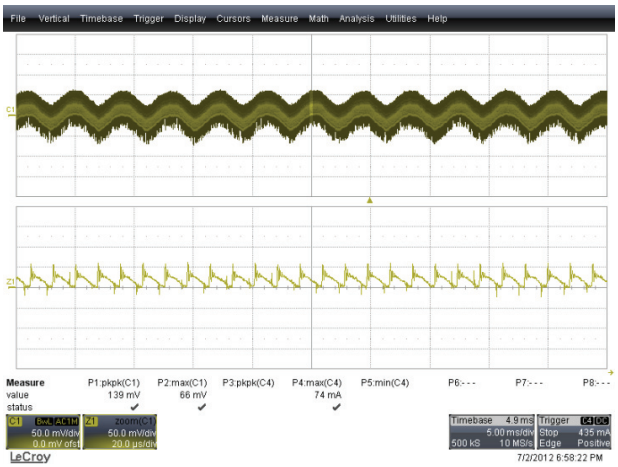

Figure 49 – 18 V_{RIPPLE}, 230 VAC, Full Load.
Upper: 18 V_{RIPPLE}, 5 ms, 50 mV / div.
Lower: 18 V_{RIPPLE}, 20 µs, 50 mV / div.

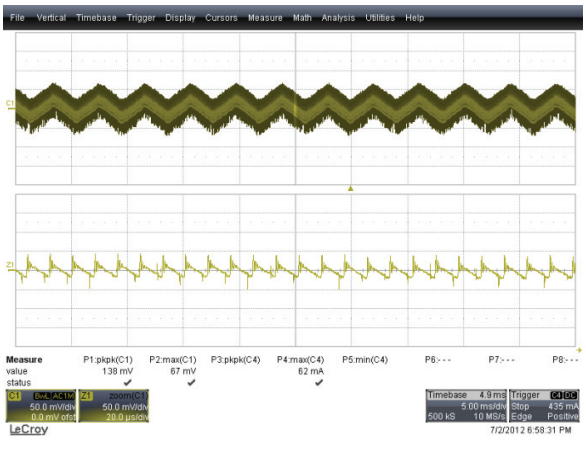

Figure 50 – 18 V_{RIPPLE}, 265 VAC, Full Load.
Upper: 18 V_{RIPPLE}, 5 ms, 50 mV / div.
Lower: 18 V_{RIPPLE}, 20 µs, 50 mV / div.

11.5.3 在18 V最大负载和5 V 1 A稳态负载下测试5 V纹波

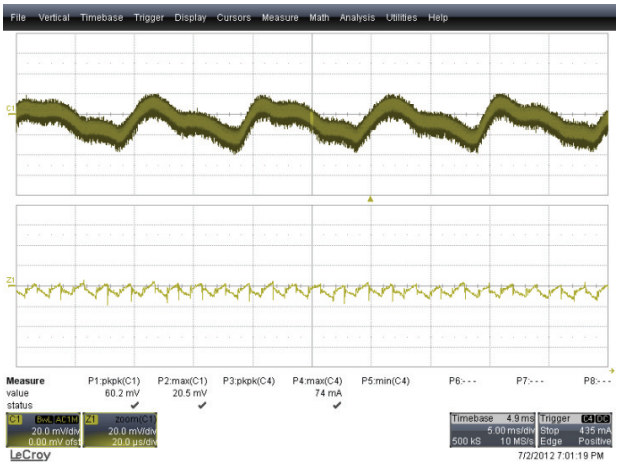

Figure 51 – Output Ripple, 90 VAC, Full Load.
Upper: 5 V_{RIPPLE}, 5 ms, 20 mV / div.
Lower: 5 V_{RIPPLE}, 20 µs, 20 mV / div.

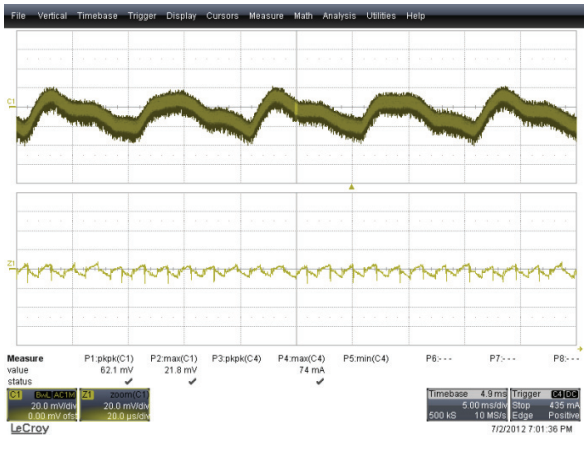

Figure 52 – Output Ripple, 115 VAC, Full Load.
Upper: 5 V_{RIPPLE}, 5 ms, 20 mV / div.
Lower: 5 V_{RIPPLE}, 20 µs, 20 mV / div.

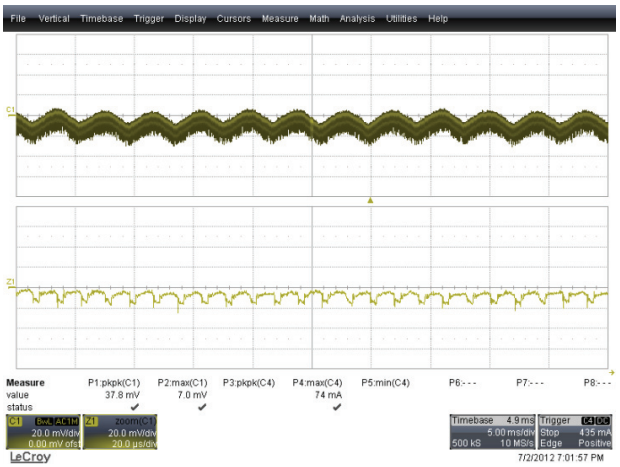

Figure 53 – Output Ripple, 230 VAC, Full Load.
Upper: 5 V_{RIPPLE}, 5 ms, 20 mV / div.
Lower: 5 V_{RIPPLE}, 20 µs, 20 mV / div.

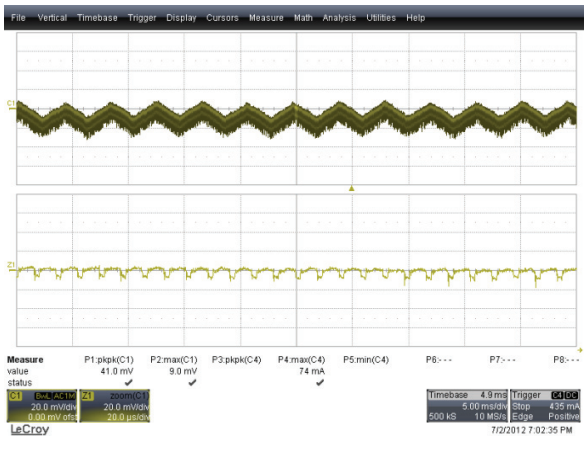

Figure 54 – Output Ripple, 265VAC, Full Load.
Upper: 5 V_{RIPPLE}, 5 ms, 20 mV / div.
Lower: 5 V_{RIPPLE}, 20 µs, 20 mV / div.

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12 保护功能

12.1 短路条件下的自动重启动

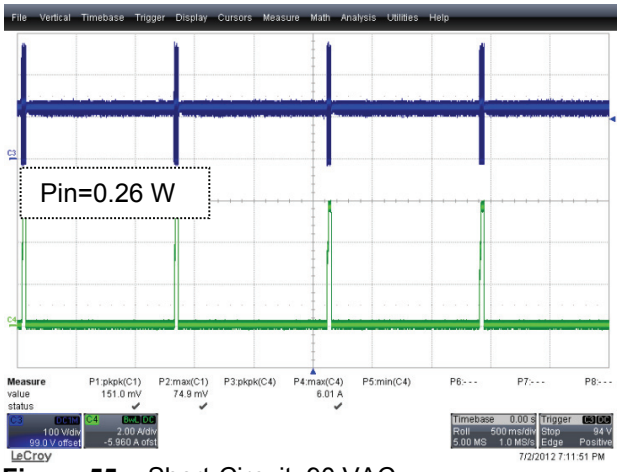

Figure 55 – Short-Circuit, 90 VAC.
Upper: V_{DS}, 100 V / div.
Lower: 5 V_{LOAD}, 500 ms, 2 A / div.

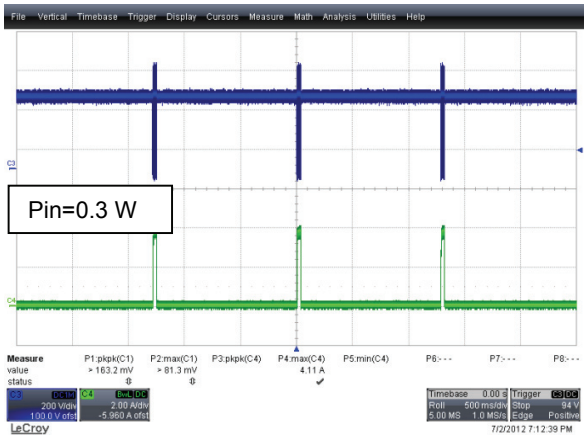

Figure 56 – Short-Circuit, 265 VAC.
Upper: V_{DS}, 200 V / div.
Lower: 5 V_{LOAD}, 500 ms, 2 A / div.

12.2 输出过压保护

Output OVP was tested by connecting a 100 kΩ resistor between CP pin and BP pin output.

Figure 57 – Output OVP, 265 VAC, Standby Load.
V_{OUT}, 5 V, 1 V, 500 ms / div.

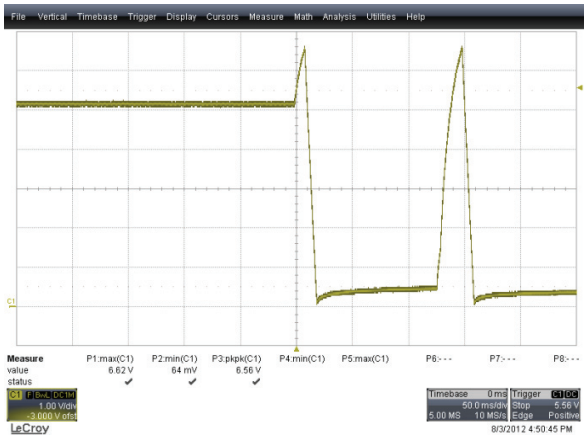

Figure 58 – Output OVP, 265 VAC, Full Load.
V_{OUT}, 5 V, 1 V, 50 ms / div.

12.3 电压缓升与电压跌落测试

At full load, AC input was transient from 0 VAC to 120 VAC for brown-in test and from 120 VAC to 0 VAC for brown-out test. Slew rate of input voltage is 12 VAC/S for brown-in and brown-out test.

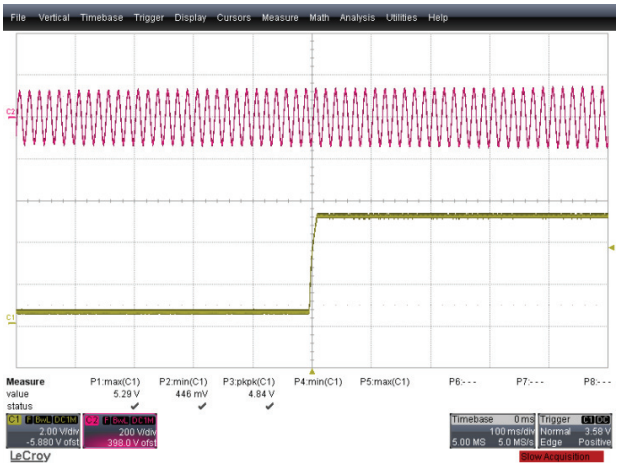

Figure 59 – Brown-In Test, Full Load.
Upper: VAC, 200 V / div.
Lower: 5 V_{OUT}, 2 V, 100 ms / div.

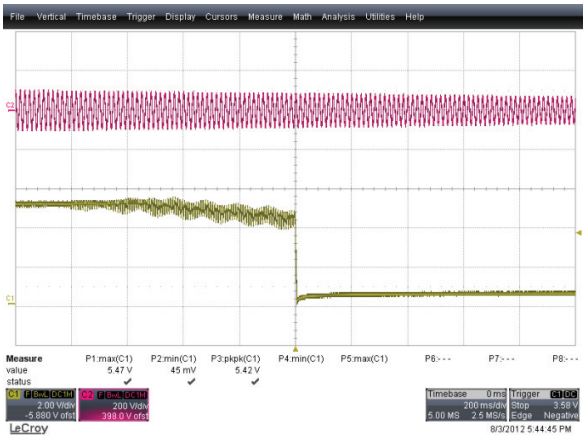

Figure 60 – Brown-In Test, Full Load.
Upper: VAC, 200 V / div.
Lower: 5 V_{OUT}, 2 V, 200 ms / div.

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13 输入浪涌

Differential input line 1.2/50 μs surge testing was conducted on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC. Resistor loads were used for both outputs (5 V/1 A and 18 V/0.67 A). Output regulation was verified after the test.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Results (Pass/Fail # Strikes)
D.M.		**(2Ù source)**		**10 Strikes each Level**
+1000	230	L1 to L2	90	Pass
–1000	230	L1 to L2	270	Pass
C.M.		**(12Ù source)**		
+2000	230	L1, L2 to PE	90	Pass
–2000	230	L1, L2 to PE	270	Pass

14 ESD

ESD passes at 8 KV for contact discharge and 15kV for air discharge, no output glitch and latch off was found during the test.

Device	Discharge Type	Discharge Location	Voltage	# of Events (1/sec)	Remarks
LNK6774V	Contact	+ Output Terminal	+8 kV	10	PASS
			-8 kV	10	PASS
		- Output Terminal	+8 kV	10	PASS
			-8 kV	10	PASS
	Air	+ Output Terminal	+15 kV	10	PASS
			-15 kV	10	PASS
		- Output Terminal	+15 kV	10	PASS
			-15 kV	10	PASS

15 满载下的EMI测试

At 115 VAC and 230 VAC, conducted emissions tests were performed at full load (0.67A DC load for 18 V and 1 A DC load for 5 V). Composite EN55022B / CISPR22B conducted limits are shown. All the tests show excellent EMI performance.

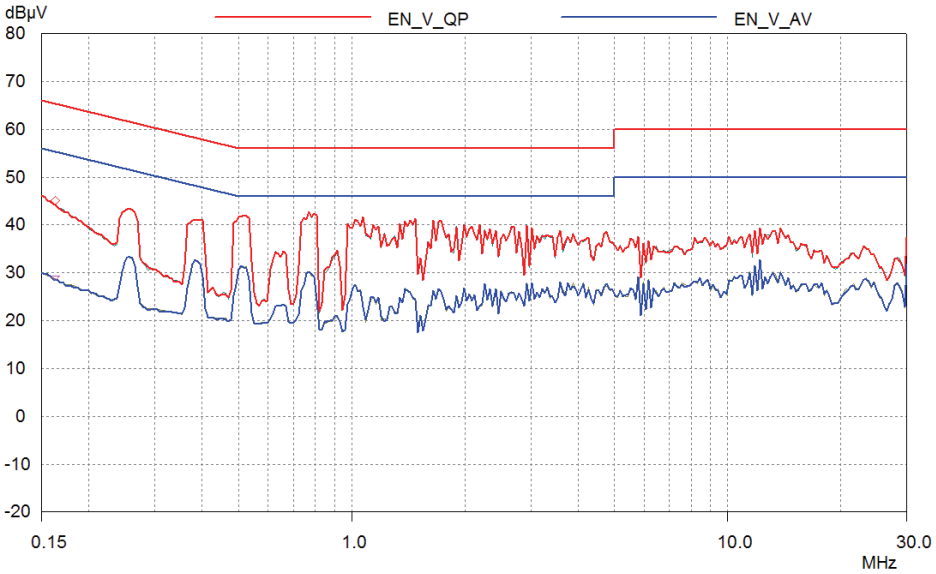

Figure 61 – Conducted EMI at 115 VAC 60 Hz, Full Load, Output Return Connected to Ground.

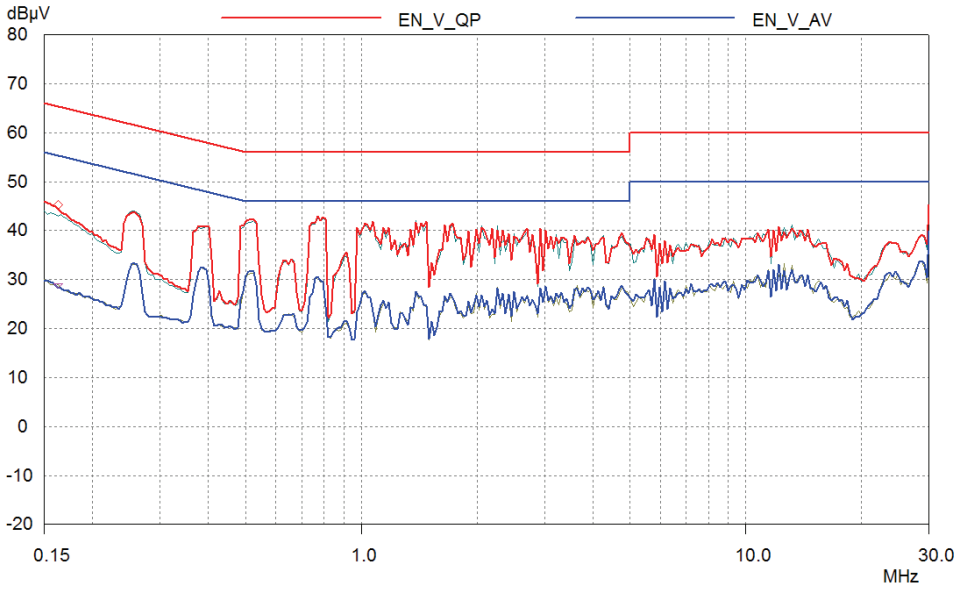

Figure 62 – Conducted EMI at 115 VAC 60 Hz, Full Load, Output Return Connected to Artificial Hand.

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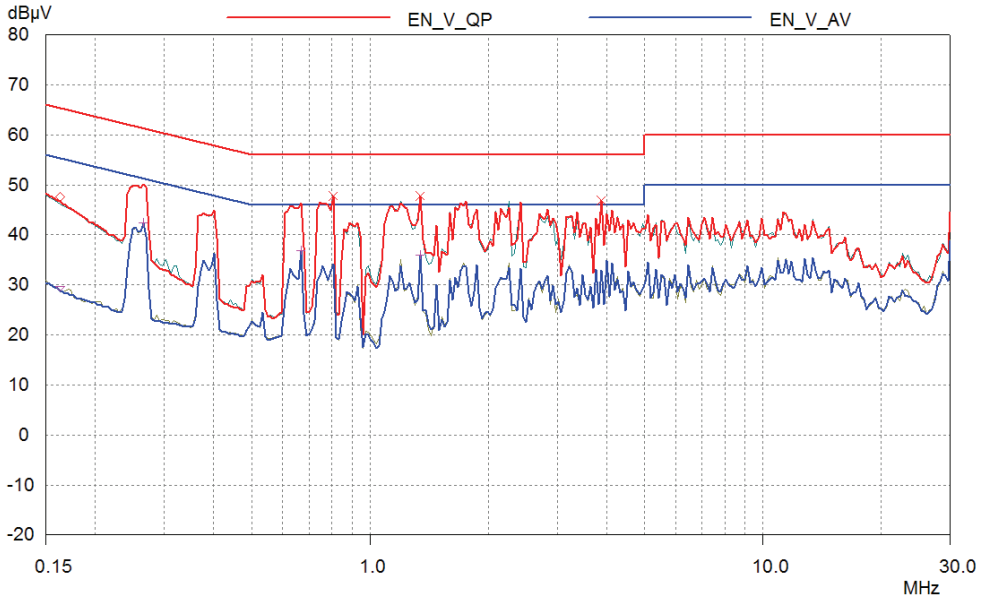

Figure 63 – Conducted EMI at 230 VAC 60 Hz, Full Load, Output Return Connected to Ground.

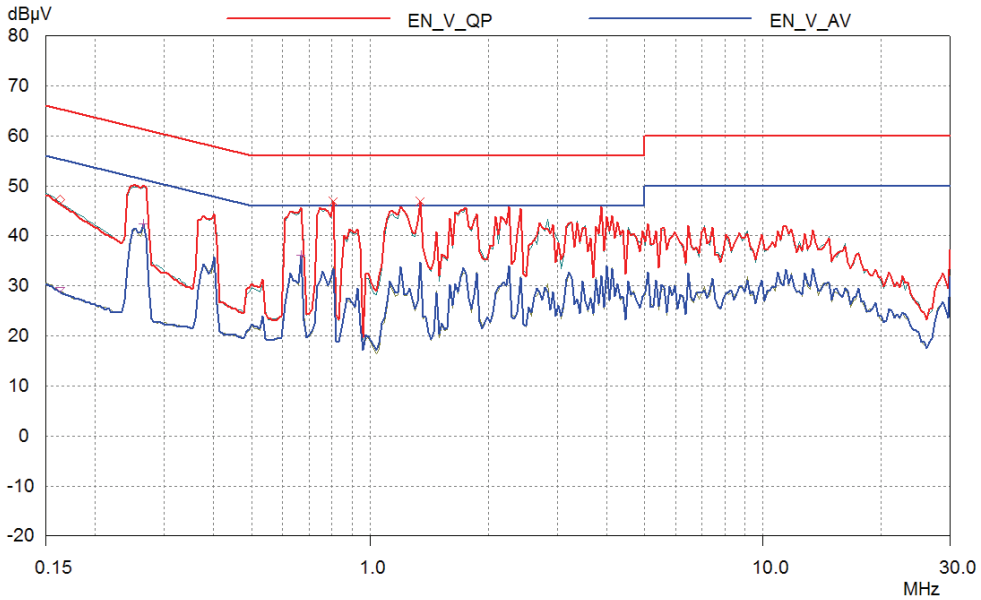

Figure 64 – Conducted EMI at 230 VAC 60 Hz, Full Load, Output Return Connected to Artificial Hand.

16 版本历史

Date	Author	Revision	Description & changes	Reviewed
28-Sep-12	KM	2.2	Initial Release	Marketing and Apps

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