Design Example Report

Title	***36 W Network Power Supply Using InnoSwitch3™-CE, INN3166C-H102***
Specification	90 VAC – 265 VAC Input; 12.0 V / 3 A Output
Application	Network Power Supply
Author	Applications Engineering Department
Document Number	DER-537
Date	July 27, 2022
Revision	1.4

Summary and Features

- Lowest cost and component count for a network power supply
- Output voltage regulation, ±5%
- Reduced dissipation during output short circuit fault
- <30 mW no-load input power
- Average efficiency at PCB >91%, and >88% at the end cable (1.8 m, #22 AWG)
- 6% cable drop compensation

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a network power supply designed to provide a nominal output voltage of 12 V at 3 A loads from a wide input voltage range of 90VAC to 265 VAC. This power supply utilizes the INN3166C from the InnoSwitch3™-CE family of devices.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

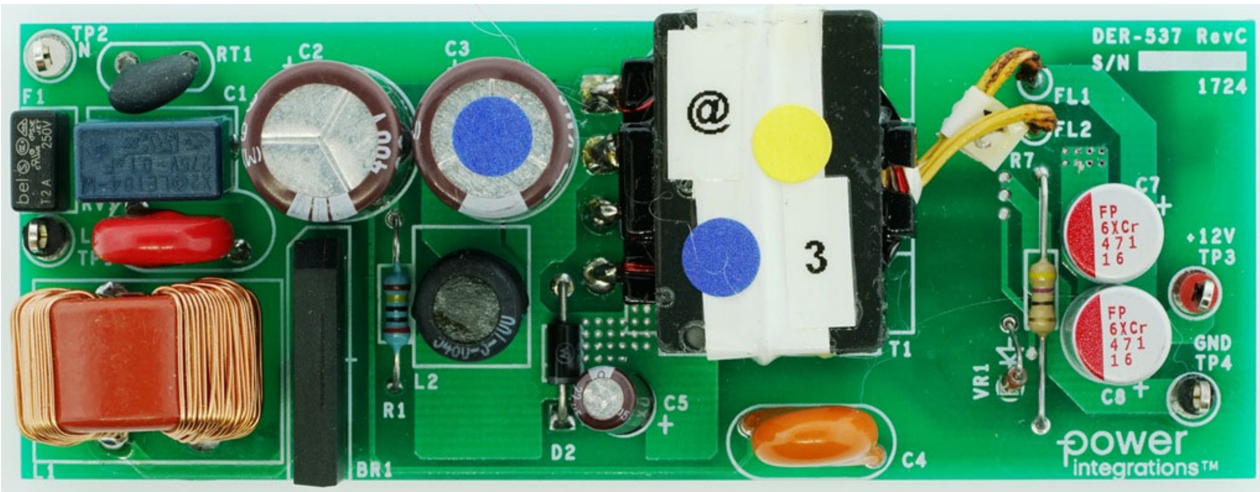


Figure 1 – Populated Circuit Board, Top View.

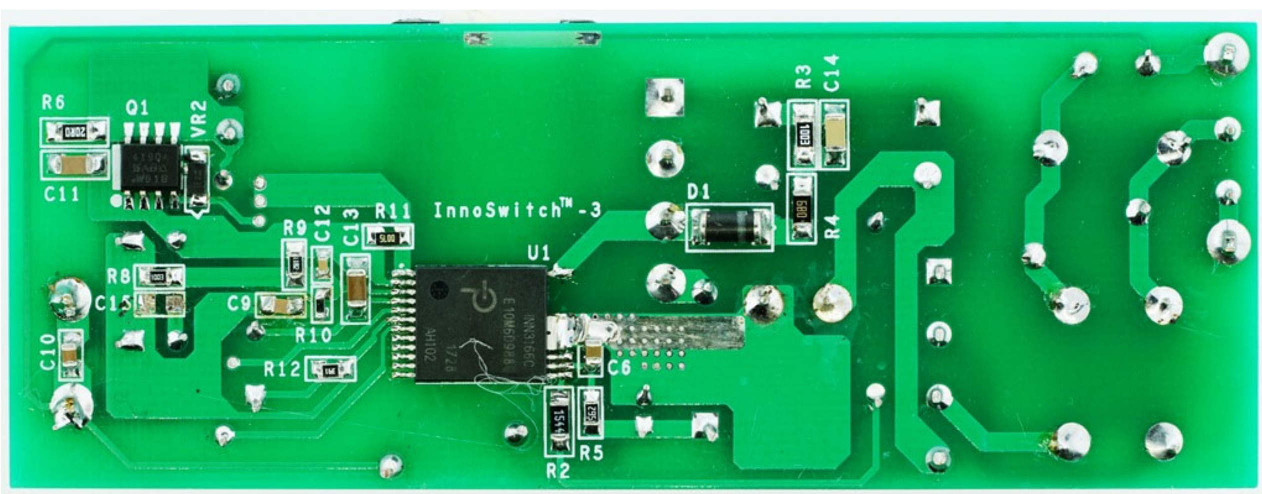


Figure 2 – Populated Circuit Board, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
No-Load Input Power				30	mW	Measured at 230 VAC Line.
Output						
Output Voltage	V_{OUT}	11.4	12	12.6	V	±5%, Measured at End of Cable. (1.8 m, #22 AWG)
Output Current	I_{OUT}	0		3	A	
Output Ripple Voltage	V_{RIPPLE}			120	mV	10 μF and 0.1 μF Capacitor. 20 MHz Bandwidth.
Rated Output Power	P_{OUT_PEAK}			36	W	
Average Efficiency 115 VAC / 230 VAC Full load	η	88			%	Measured at end of Cable. (1.8 m, #22 AWG)
Environmental						
Conducted EMI		CISPR22B / EN55022B Load floating				Resistive Load.
Line Surge Differential mode Common mode				 2 3	 kV kV	IEC61000-4-5.
Ambient Temperature	T_{AMB}	0		45	ºC	Free Convection, Sea Level in Sealed Enclosure.

3 Schematic

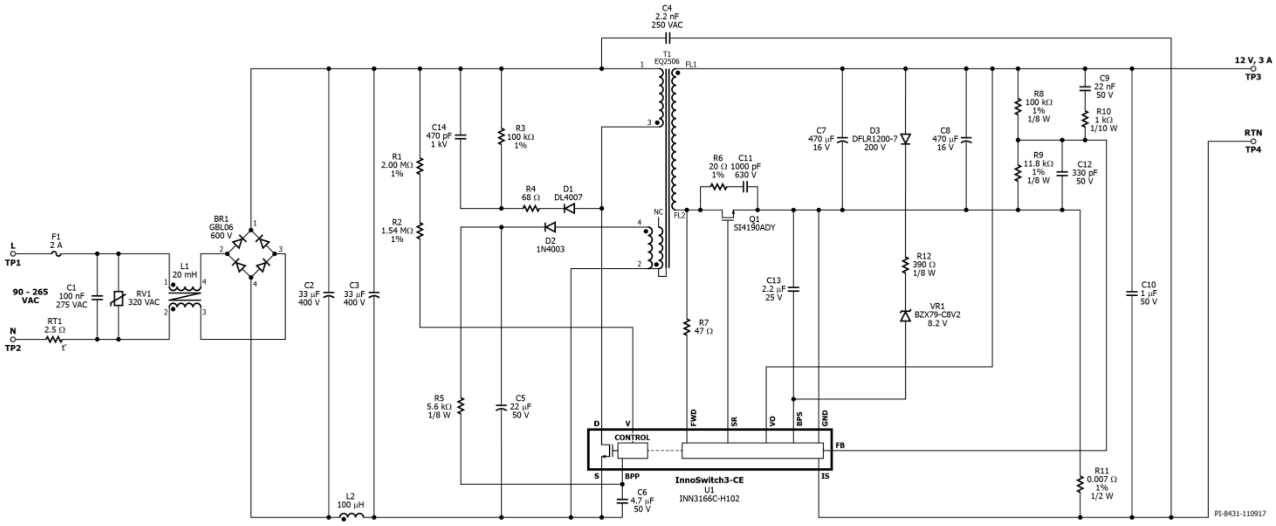


Figure 3 – Schematic.

4 Circuit Description

4.1 Filter and Input Rectifier

Fuse F1 provides protection against catastrophic failure. Thermistor RT1 limits inrush current on the power supply and a varistor RV1 provides protection from a line surge event. An X-capacitor C1 and common mode choke L1 provides filter to attenuate common mode noise. A Bridge rectifier BR1 rectifies the input supply and charges the bulk storage capacitors C2 and C3. Capacitors C2 and C3 also provide filtering of the rectified AC input and together with L2 form a π (pi) filter to attenuate differential mode noise.

4.2 INN3166C Primary and Auxiliary Section

A flyback topology was utilized on this design. One side of the transformer T1 is connected to the rectified DC bus and the other side is connected to the integrated 650 V power MOSFET inside of INN3166C IC (U1).

A low cost RCD clamp formed by D1, R3, R4, and C14 limits the peak Drain voltage due to the effects of transformer leakage reactance and output trace inductance.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C6, when AC is applied. During normal operation the primary-side block was powered from an auxiliary winding of the transformer. The output of the bias winding was rectified and filtered using diode D2 and capacitor C5. In the event of overvoltage at output, the increased voltage at the output of the bias winding cause the Zener diode VR2 to conduct and triggers the OVP protection in the primary-side controller of the INN3166C IC. Diode D3 prevents any reverse current flowing from BPP capacitor to the bias capacitor during start-up time. Resistor R5 and R13 limit current into BPP capacitor from the bias capacitor.

Resistors R1 and R2 provide line voltage sensing and provide a current to U1, which is proportional to the DC voltage across capacitor C3. At approximately 90 VDC, the current through these resistors exceeds the line undervoltage threshold, which results in enabling of U1. At approximately 415 VAC, the current through these resistors exceeds the line overvoltage threshold, which results in disabling of U1.

4.3 INN3166C Secondary Section

The secondary side of the INN3166C provides output voltage, output current sensing, output voltage protection and drive to a MOSFET providing synchronous rectification.

Output rectification for the 12 V output is provided by SR FET Q1. A RC snubber network comprising R6 and C11 for Q1 damps high frequency ringing across the SR FET, which results from leakage inductance of the transformer windings and the secondary trace inductances. The gate of Q1 is turned on based on the winding voltage sensed via R7 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below ground. Secondary-side control of the primary-side MOSFET ensures that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR pin. The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, fed into the VO pin and charges the decoupling capacitor C13 via an internal regulator. The OVP sensing Zener diode, VR1, provides secondary side output over voltage protection with R12. Feed forward RC networks comprising capacitor C9 and resistor R10 reduce the output ripple voltage.

Resistors R8 and R9 form a voltage divider network that senses the output voltage. INN3166C IC has an internal reference of 1.266 V. Capacitor C12 provides decoupling from high frequency noise affecting power supply operation. The output current is sensed by R11 with a threshold of approximately 33 mV to reduce losses. Once the current sense threshold across these resistors is exceeded, the device adjusts the number of switch pulses to maintain a fixed output current. Capacitor C10 reduces radiation EMI noise.

5 PCB Layout

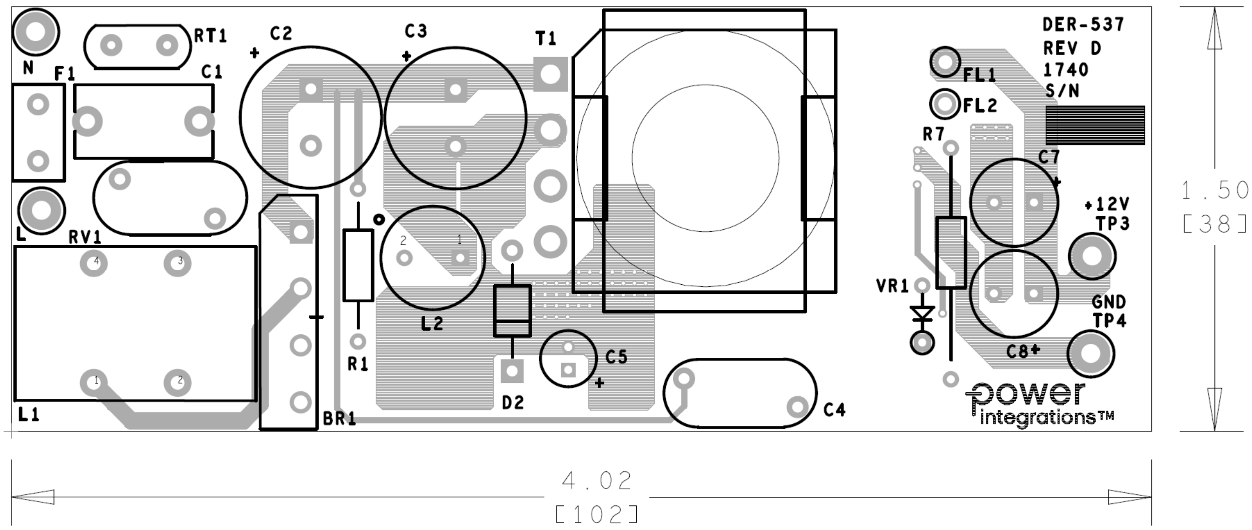


Figure 4 – Top Side.

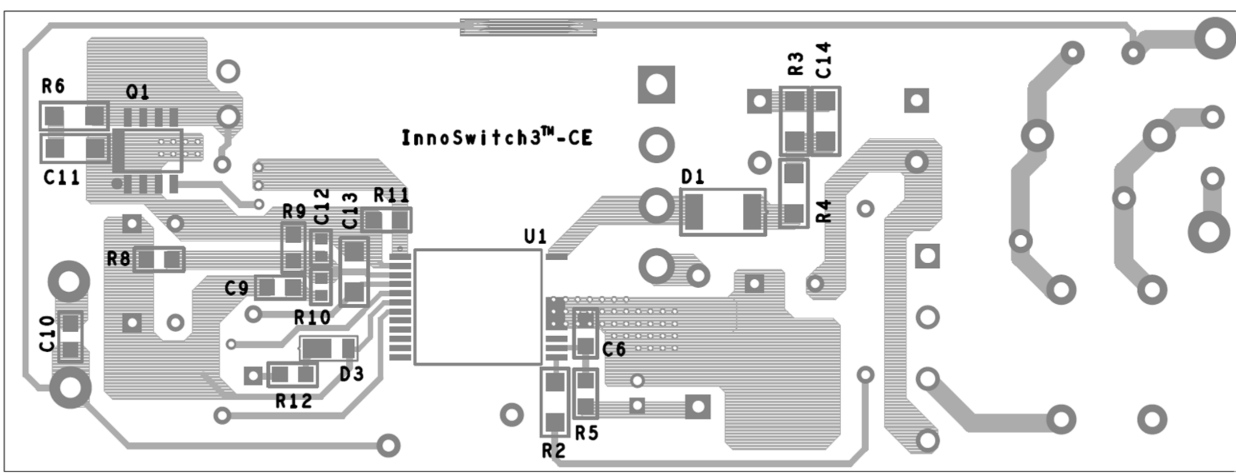


Figure 5 – Bottom Side.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	DIODE BRIDGE 600 V 4 A GB	GBL06	Genesic Semi
2	1	C1	100 nF, 275 VAC, Film, X2	LE104-M	OKAYA
3	2	C2 C3	33 μF, 400 V, Electrolytic, (12.5 x 20)	KMG401ELL330MK20S	Nippon Chemi-Con
4	1	C4	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
5	1	C5	22 μF, 50 V, Electrolytic, Very Low ESR, 340 mΩ, (5 x 11)	EKZE500ELL220ME11D	Nippon Chemi-Con
6	1	C6	4.7 μF, 50 V, Ceramic, X5R, 0805	CL21A475KBQNNNE	Samsung
7	2	C7 C8	470 μF, 16 V, Al Organic Polymer, 12 mΩ, (8 x 11.5)	RNE1C471MDN1	Nichicon
8	1	C9	22 nF 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB223	Yageo
9	1	C10	1 μF,50 V, Ceramic, X7R, 0805	C2012X7R1H105M085AC	TDK
10	1	C11	1000 pF, 630 V, Ceramic, X7R, 1206	C1206C102KBRACTU	Kemet
11	1	C12	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
12	1	C13	2.2 μF, 25 V, Ceramic, X7R, 1206	TMK316B7225KL-T	Taiyo Yuden
13	1	C14	470 pF, 1000 V, Ceramic, COG, 1206	VJ1206A471JXGAT5Z	Vishay
14	1	D1	1000 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4007-13-F	Diodes, Inc.
15	1	D3	DIODE GP 200 V 1 A POWERDI123	DFLR1200-7	Diodes, Inc.
16	1	D2	200 V, 1 A, Rectifier, DO-41	1N4003RLG	On Semi
17	1	F1	2 A, 250 V, Slow, Long Time Lag, RST	RST 2	Belfuse
18	1	L1	20 mH,30%, 1.5A, 270 mΩ, 250 VAC max, 2LN, TH	744823220 TSD-4091	Wurth Premier Magnetics
19	1	L2	100 μH, 1.0 A, 20%	RL-5480-3-100 PM-R39101	Renco Premier Magnetics
20	1	Q1	MOSFET, N-Channel, 100 V, 18.4 A, SO-8	SI4190ADY-T1-GE3	Vishay
21	1	R1	RES, 2.00 MΩ, 1%, 1/4 W, Metal Film	RNF14FTD2M00	Stackpole
22	1	R2	RES, 1.54 MΩ, 1%, 1/4 W, Thick Film, 1206	CRCW12061M54FKEA	Vishay
23	1	R3	RES, 100 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1003V	Panasonic
24	1	R4	RES, 68 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ680V	Panasonic
25	1	R5	RES, 5.6 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ562V	Panasonic
26	1	R6	RES, 20 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF20R0V	Panasonic
27	1	R7	RES, 47 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-47R	Yageo
28	1	R8	RES, 100 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1003V	Panasonic
29	1	R9	RES, 11.8 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1182V	Panasonic
30	1	R10	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
40	1	R11	RES, 0.007 Ω, ±1%, 1/2 W, 0805, Current Sense,	PMR10EZPFU7L00	Rohm
41	1	R12	RES, 390 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ391V	Panasonic
42	1	RT1	NTC Thermistor, 2.5 Ω, 3 A	SL08 2R503	Ametherm
43	1	RV1	320 VAC, 23 J, 10 mm, RADIAL	V320LA10P	Littlefuse
44	1	T1	Bobbin, EQ2506, 4 pins, 4pri, 0sec Transformer	EQ-27 POL-INN028	Shen Zhen Xin Yu Jia Tech Premier Magnetics
45	1	U1	InnoSwitch3-CE	INN3166C-H102	Power Integrations
46	1	VR1	8.2 V, 500 mW, 5%, DO-35	BZX79-C8V2,133	NXP Semi

7 Transformer Specification

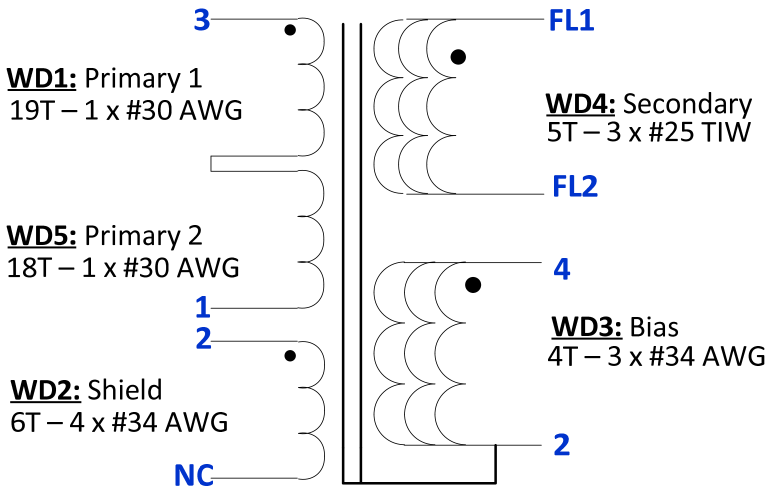


Figure 6 – Transformer Electrical Diagram.

7.1 Electrical Specifications

Electrical Strength	60 Hz 1 second, from pins 1, 2, 3, 4 to pins FL1, FL2.	3000 VAC
Primary Inductance	Measured at 1 V_{PK-PK}, typical switching frequency, between pin 1 to pin 3, with all other windings open.	910 μH ±5%
Primary Leakage Inductance	Pins 1-3, with Pins 2-4, FL1-FL2 shorted, measured at 100 kHz, 0.4 V_{RMS}.	22.74 μH (Max.)

7.2 Material List

Item	Description
[1]	Core: EQ27, Shen Zhen Xin Yu Tech Ltd.
[2]	Bobbin: EQ2506-V-4 pins (4/0); Shen Zhen Xin Yu Tech Ltd., PI#: 25-01095-00.
[3]	Magnet Wire: #30 AWG, Double Coated.
[4]	Magnet Wire: #34 AWG, Double Coated.
[5]	Magnet Wire: #25 AWG, Triple Insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 4.5 mm Wide.
[7]	Coil Tape: 1 mil Thick, 6 mm Wide.
[8]	Varnish: Dolph BC-359.

7.3 Transformer Build Diagram

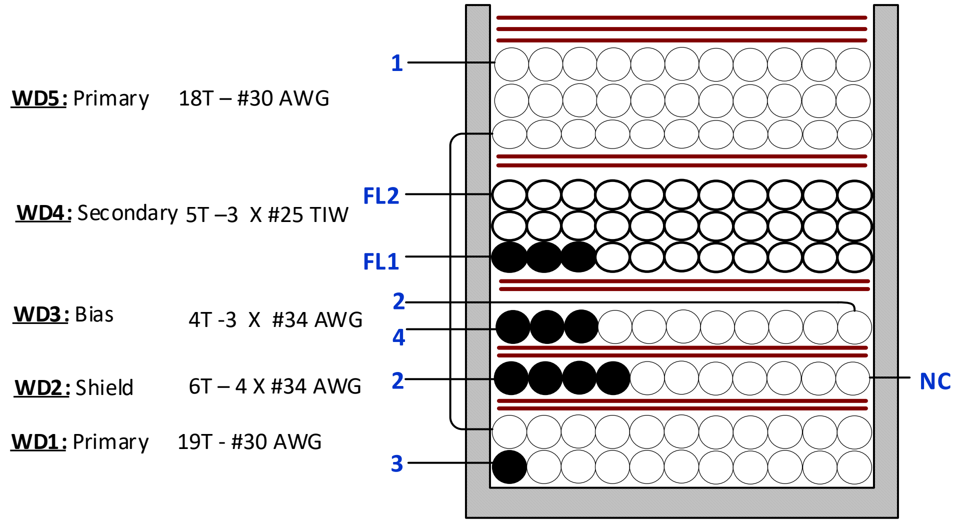
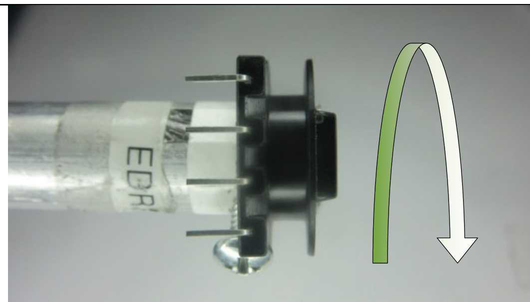
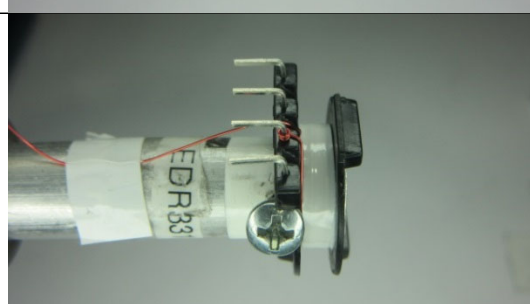
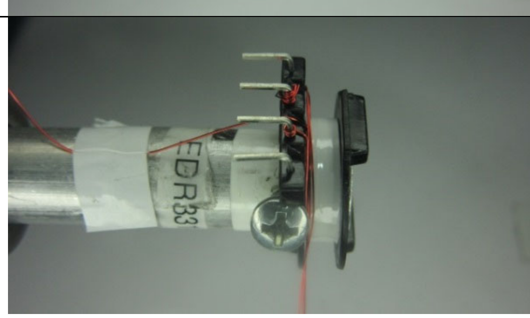


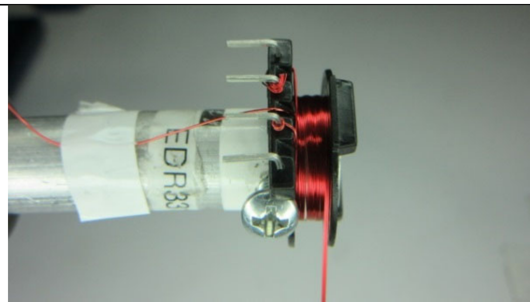
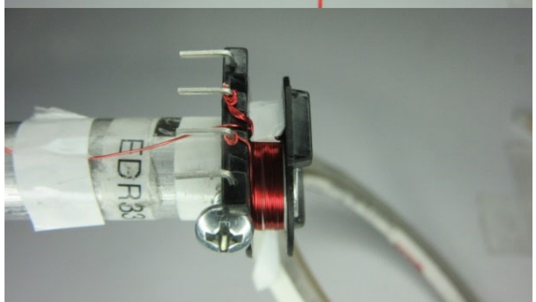
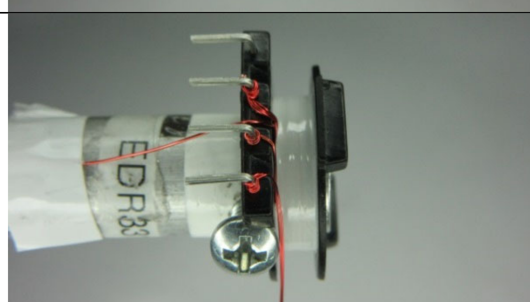
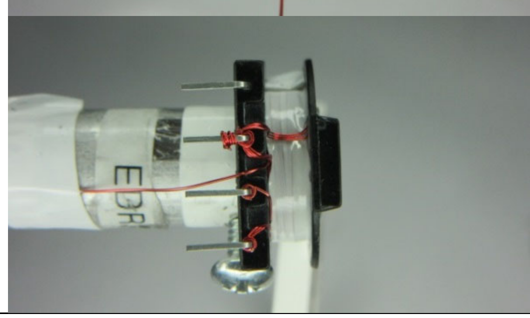
Figure 7 – Transformer Build Diagram.

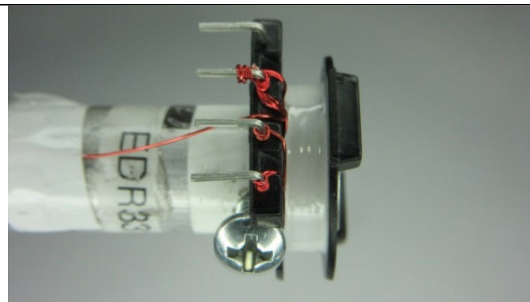
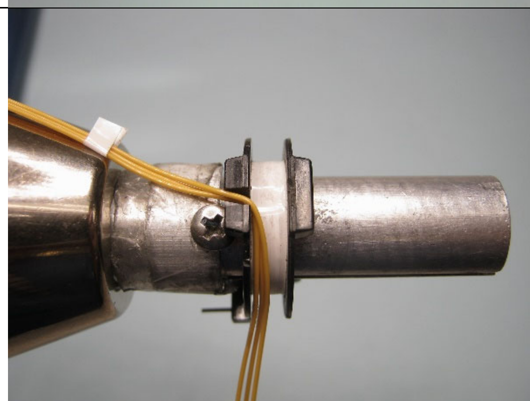
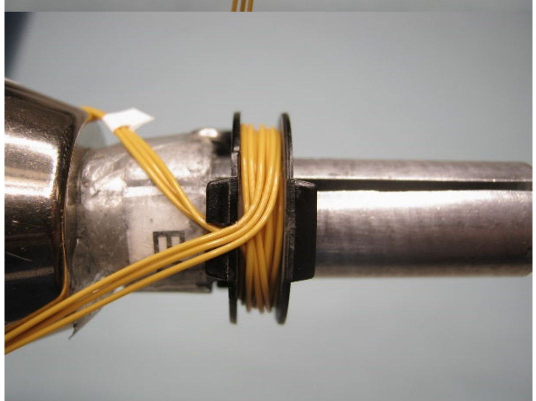
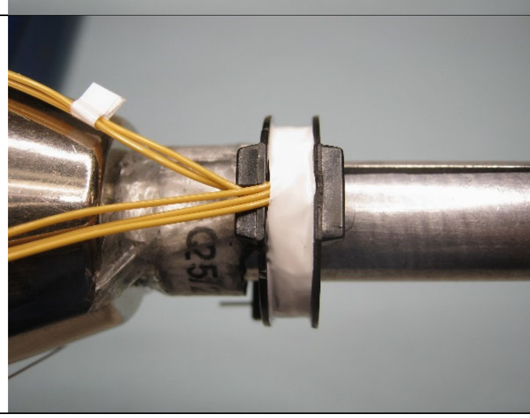
7.4 Transformer Instructions

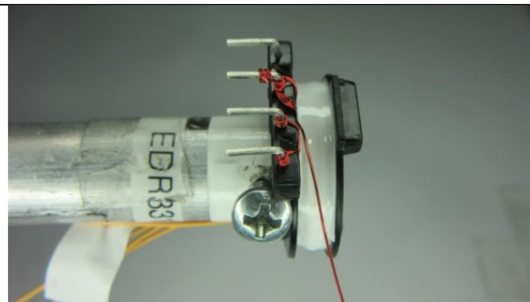
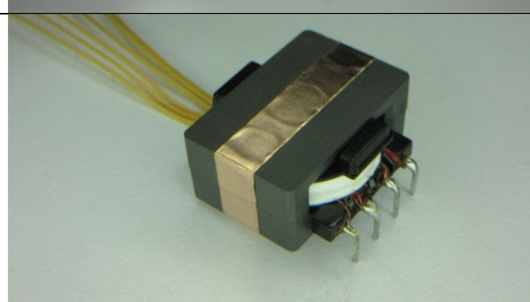
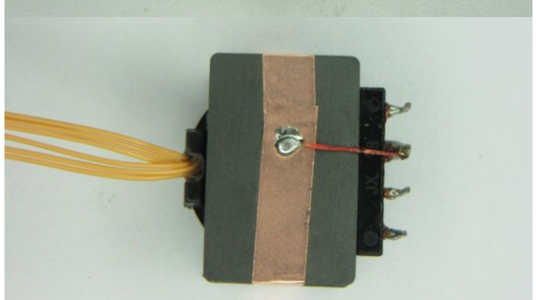
Winding Preparation	For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
WD1 Primary	Start on pin(s) 3 and wind 19 turns (x 1 filar) of Item [3]. In 2 layers from left to right. On the final layer, spread the winding evenly across entire bobbin. Don't terminate.
Insulation	Add 2 layer of tape, Item [6], for insulation.
WD2 Shield	Start on pin(s) 2 and wind 6 turns (x 4 filar) of Item [4]. Wind in same rotational direction as primary winding. Spread the winding evenly across entire bobbin. Terminate after finish. Leave this end of shield winding not connected.
Insulation	Add 2 layer of tape, Item [6], for insulation.
WD3 Bias	Start on pin(s) 4 and wind 4 turns (x 3 filar) of Item [4]. Wind in same rotational direction as primary winding. Spread the winding evenly across entire bobbin. Finish this winding on pin(s) 2.
Insulation	Add 2 layers of tape, Item [6], for insulation.
WD4 Secondary	Start on pin(s) FL1 and wind 5 turns (x 3 filar) of Item [5]. Spread the winding evenly across entire bobbin. Wind in clockwise direction. Finish this winding on pin(s) FL2.
Insulation	Add 2 layers of tape, Item [6], for insulation.
WD5 Primary	Continue WD1. Wind 18 turns (x 1 filar) of Item [3]. In 2 layer(s) from left to right. On the final layer, spread the winding evenly across entire bobbin. Finish this winding on pin(s) 1.
Insulation	Add 3 layers of tape, Item [6], for insulation.
Assembly	Gap core halves for 910 μH inductance. Assemble and secure core halves. Item [1].
Flux Band	On the core, wrap around Item [7]. Connect (x 3 filar) of Item [4] from band to pin(s) 2. Add 2 layers of tape, Item [6], for insulation.
Finish	Dip varnish uniformly in Item [8]. Do not vacuum impregnate.

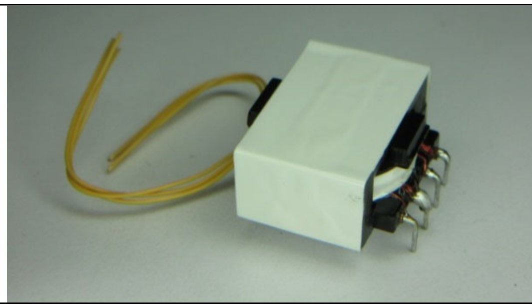
7.5 Transformer Winding Illustrations

Winding Preparation		For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
WD1: Primary	 	Start on pin(s) 3 and wind 19 turns (x 1 filar) of Item [3]. In 2 layers from left to right. On the final layer, spread the winding evenly across entire bobbin. Don't terminate.
Insulation		Add 2 layer of tape, Item [6], for insulation.
WD2: Shield		Start on pin(s) 2 and wind 6 turns (x 4 filar) of Item [4]. Wind in same rotational direction as primary winding. Spread the winding evenly across entire bobbin. Terminate after finish. Leave this end of shield winding not connected.

	 	
Insulation		Add 2 layers of tape, Item [6], for insulation.
WD3: **Bias**	 	Start on pin(s) 4 and wind 4 turns (x 3 filar) of Item [4]. Wind in same rotational direction as primary winding. Spread the winding evenly across entire bobbin. Finish this winding on pin(s) 2.

Insulation		Add 2 layers of tape, Item [6], for insulation.
WD4: Secondary	 	Start on pin(s) FL1 and wind 5 turns (x 3 filar) of Item [5]. Spread the winding evenly across entire bobbin. Wind in clockwise direction. Finish this winding on pin(s) FL2.
Insulation		Add 2 layers of tape, Item [6], for insulation.

WD5: Primary	 	Continue WD1. Wind 18 turns (x 1 filar) of Item [3]. In 2 layer(s) from left to right. On the final layer, spread the winding evenly across entire bobbin. Finish this winding on pin(s) 1.
Insulation		Add 3 layers of tape, Item [6], for insulation.
Flux Band	 	On the core, wrap around Item [7]. Connect (x 3 filar) of Item [4] from band to pin(s) 2. Add 2 layers of tape, Item [6], for insulation.

Finish		Dip varnish uniformly in Item [8]. Do not vacuum impregnate.

8 Transformer Design Spreadsheet

ACDC_InnoSwitch3-CE_Flyback_083017; Rev.1.0; Copyright Power Integrations 2017	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3 CE Flyback Design Spreadsheet
APPLICATION VARIABLES					
VIN_MIN	90		90	V	Minimum AC input voltage
VIN_MAX			265	V	Maximum AC input voltage
VIN_RANGE			UNIVERSAL		Range of AC input voltage
LINEFREQ			60	Hz	AC Input voltage frequency
CAP_INPUT	66.0		66.0	uF	Input capacitor
VOUT	12.00		12.36	V	Output voltage at the board
PERCENT_CDC	3%	Info	3%		Refer to the device H-code in the datasheet to ensure that the desired H-code is available for the device selected
IOUT	3.00		3.00	A	Output current
POUT		Info	37.08	W	The specified output power exceeds the device power capability: Verify thermal performance
EFFICIENCY	0.85		0.85		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
FACTOR_Z	0.50		0.50		Z-factor estimate
ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
PRIMARY CONTROLLER SELECTION					
ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
DEVICE_GENERIC	INN31X6		INN31X6		Generic device code
DEVICE_CODE			INN3166C		Actual device code
POUT_MAX			27	W	Power capability of the device based on thermal performance
RDSON_100DEG			2.53	Ω	Primary MOSFET on time drain resistance at 100 degC
ILIMIT_MIN			1.32	A	Minimum current limit of the primary MOSFET
ILIMIT_TYP			1.45	A	Typical current limit of the primary MOSFET
ILIMIT_MAX			1.58	A	Maximum current limit of the primary MOSFET
VDRAIN_BREAKDOWN			650	V	Device breakdown voltage
VDRAIN_ON_MOSFET			1.16	V	Primary MOSFET on time drain voltage
VDRAIN_OFF_MOSFET			535.4	V	Peak drain voltage on the primary MOSFET during turn-off
WORST CASE ELECTRICAL PARAMETERS					
FSWITCHING_MAX	71500		71500	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
VOR	92.0		92.0	V	Seconday voltage reflected to the primary when the primary MOSFET turns off
VMIN			89.25	V	Valley of the rectified minimum AC input voltage at full power
KP			0.57		Measure of continuous/discontinuous mode of operation
MODE_OPERATION			CCM		Mode of operation
DUTYCYCLE			0.511		Primary MOSFET duty cycle
TIME_ON			10.89	us	Primary MOSFET on-time
TIME_OFF			6.84	us	Primary MOSFET off-time
LPRIMARY_MIN			844.9	uH	Minimum primary inductance
LPRIMARY_TYP			889.4	uH	Typical primary inductance
LPRIMARY_TOL	5.0		5.0	%	Primary inductance tolerance
LPRIMARY_MAX			933.9	uH	Maximum primary inductance
PRIMARY CURRENT					
IPEAK_PRIMARY			1.43	A	Primary MOSFET peak currrent
IPEDESTAL_PRIMARY			0.54	A	Primary MOSFET current pedestal
IAVG_PRIMARY			0.46	A	Primary MOSFET average current
IRIPPLE_PRIMARY			1.07	A	Primary MOSFET ripple current

IRMS_PRIMARY			0.68	A	Primary MOSFET RMS current
SECONDARY CURRENT					
IPEAK_SECONDARY			10.58	A	Secondary winding peak current
IPEDESTAL_SECONDARY			3.97	A	Secondary winding current pedestal
IRMS_SECONDARY			5.42	A	Secondary winding RMS current
TRANSFORMER CONSTRUCTION PARAMETERS					
CORE SELECTION					
CORE	Custom		Custom		Core selection
CORE CODE	EQ27		EQ27		Core code
AE	108.00		108.00	mm^2	Core cross sectional area
LE	36.30		36.30	mm	Core magnetic path length
AL	7700		7700	nH/turns^2	Ungapped core effective inductance
VE	3920.0		3920.0	mm^3	Core volume
BOBBIN	ER2506		ER2506		Bobbin
AW	62.00		62.00	mm^2	Window area of the bobbin
BW	4.25		4.25	mm	Bobbin width
MARGIN	0.0		0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
PRIMARY WINDING					
NPRIMARY			37		Primary turns
BPEAK			3782	Gauss	Peak flux density
BMAX			3296	Gauss	Maximum flux density
BAC			945	Gauss	AC flux density
ALG			650	nH/turns^2	Typical gapped core effective inductance
LG			0.191	mm	Core gap length
LAYERS_PRIMARY	4		4		Number of primary layers
AWG_PRIMARY			27	AWG	Primary winding wire AWG
OD_PRIMARY_INSULATED			0.418	mm	Primary winding wire outer diameter with insulation
OD_PRIMARY_BARE			0.361	mm	Primary winding wire outer diameter without insulation
CMA_PRIMARY			297	Cmil/A	Primary winding wire CMA
SECONDARY WINDING					
NSECONDARY	5		5		Secondary turns
AWG_SECONDARY			20	AWG	Secondary winding wire AWG
OD_SECONDARY_INSULATED			1.118	mm	Secondary winding wire outer diameter with insulation
OD_SECONDARY_BARE			0.812	mm	Secondary winding wire outer diameter without insulation
CMA_SECONDARY			208	Cmil/A	Secondary winding wire CMA
BIAS WINDING					
NBIAS			6		Bias turns
PRIMARY COMPONENTS SELECTION					
Line undervoltage					
BROWN-IN REQURED			76.5	V	Required AC RMS line voltage brown-in threshold
RLS			4.52	MΩ	Connect two 2.26 MOhm resistors to the V-pin for the required UV/OV threshold
BROWN-IN ACTUAL			77.0	V	Actual AC RMS brown-in threshold
BROWN-OUT ACTUAL			70.6	V	Actual AC RMS brown-out threshold
Line overvoltage					
OVERVOLTAGE_LINE			339.2	V	Actual AC RMS line over-voltage threshold
Bias diode					
VBIAS			12.0	V	Rectified bias voltage
VF_BIAS			0.70	V	Bias winding diode forward drop
VREVERSE_BIASDIODE			72.55	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
CBIAS			22	uF	Bias winding rectification capacitor
CBPP			4.70	uF	BPP pin capacitor
SECONDARY COMPONENTS					
RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)

RFB_LOWER			11.50	kΩ	Lower feedback resistor
CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
MULTIPLE OUTPUT PARAMETERS					
OUTPUT 1					
VOUT1			12.36	V	Output 1 voltage
IOUT1	3.00		3.00	A	Output 1 current
POUT1			37.08	W	Output 1 power
IRMS_SECONDARY1			4.91	A	Root mean squared value of the secondary current for output 1
IRIPPLE_CAP_OUTPUT1			3.88	A	Current ripple on the secondary waveform for output 1
AWG_SECONDARY1			20	AWG	Wire size for output 1
OD_SECONDARY1_INSULATED			1.118	mm	Secondary winding wire outer diameter with insulation for output 1
OD_SECONDARY1_BARE			0.812	mm	Secondary winding wire outer diameter without insulation for output 1
CM_SECONDARY1			981	Cmils	Bare conductor effective area in circular mils for output 1
NSECONDARY1			5		Number of turns for output 1
VREVERSE_RECTIFIER1			62.81	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
SRFET1	Auto		AOD2816		SRFET selection for output 1
VF_SRFET1			0.087	V	SRFET on-time drain voltage for output 1
VBREAKDOWN_SRFET1			80	V	SRFET breakdown voltage for output 1
RDSON_SRFET1			29.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
TOLERANCE ANALYSIS					
CORNER_VAC			90	V	Input AC RMS voltage corner to be evaluated
CORNER_ILIMIT	TYP		1.45	A	Current limit corner to be evaluated
CORNER_LPRIMARY	TYP		889.4	uH	Primary inductance corner to be evaluated
MODE_OPERATION			CCM		Mode of operation
KP			0.666		Measure of continuous/discontinuous mode of operation
FSWITCHING			56563	Hz	Switching frequency at full load and valley of the rectified minimum AC input voltage
DUTYCYCLE			0.511		Steady state duty cycle
TIME_ON			9.03	us	Primary MOSFET on-time
TIME_OFF			8.65	us	Primary MOSFET off-time
IPEAK_PRIMARY			1.34	A	Primary MOSFET peak currrent
IPEDESTAL_PRIMARY			0.45	A	Primary MOSFET current pedestal
IAVERAGE_PRIMARY			0.46	A	Primary MOSFET average current
IRIPPLE_PRIMARY			0.89	A	Primary MOSFET ripple current
IRMS_PRIMARY			0.67	A	Primary MOSFET RMS current
CMA_PRIMARY			302	Cmil/A	Primary winding wire CMA
BPEAK			3303	Gauss	Peak fux density
BMAX			2991	Gauss	Maximum flux density

9 Performance Data

9.1 Full Load Efficiency vs. Input Line Voltage (at PCB)

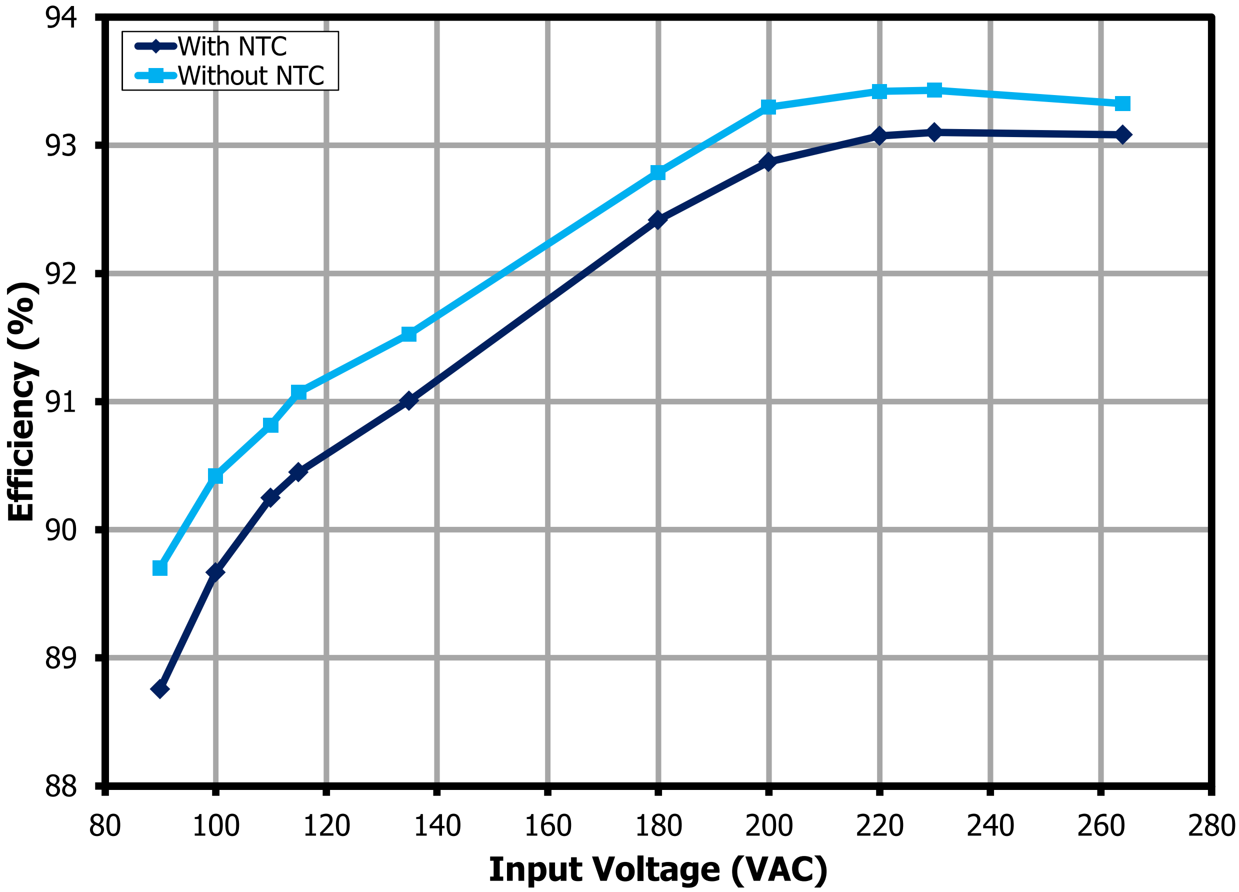


Figure 8 – Efficiency vs. Line Voltage, Room Temperature Measured at End of Cable.

9.2 Efficiency vs. Load (at PCB)

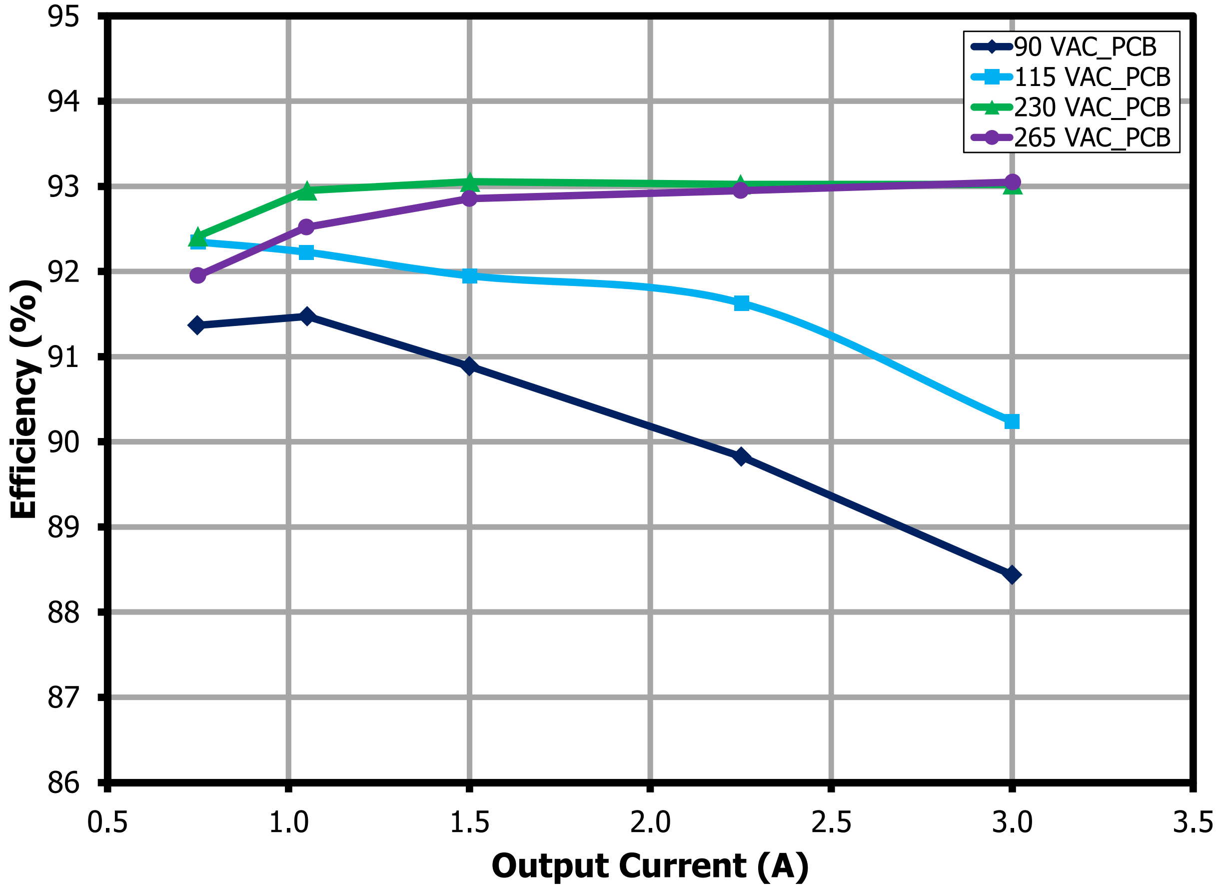


Figure 9 – Efficiency vs. Load, Room Temperature Measured at PCB.

9.3 Average Efficiency at the end of cable

Requirement	Minimum Average Efficiency (%)		Maximum Power in No-Load Mode (W)
DOE VI	≥ 0.071 x ln(Pout) – 0.0014 x Pout + 0.67	87.4%	≤ 0.100
CoC Tier 1	≥ 0.0626 x ln(Pout) + 0.646	87.0%	≤ 0.150

9.4 At 115 VAC / 60 Hz

Load (A) (%)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency at PCB (%)	V_{OUT} at End 1.8 m, #22 AWG Cable (0.2 Ω)	Efficiency at End of Cable (%)
100	114.96	0.66	41.69	12.54	3.00	37.62	90.24	11.94	86
75	114.97	0.51	30.53	12.42	2.25	27.97	91.63	11.97	88
50	114.98	0.36	20.20	12.38	1.50	18.57	91.95	12.08	90
25	114.98	0.20	9.95	12.25	0.75	9.19	92.35	12.10	91
						Average	**91.54**		**88.79**

9.5 At 230 VAC / 50 Hz

Load (A) (%)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency at PCB (%)	V_{OUT} at End 1.8 m, #22 AWG Cable (0.2 Ω)	Efficiency at End of Cable (%)
100	229.91	0.41	40.83	12.65	3.00	37.98	93.02	12.05	89
75	229.92	0.32	30.35	12.55	2.25	28.23	93.02	12.10	90
50	229.92	0.23	20.07	12.44	1.50	18.68	93.05	12.13	91
25	229.92	0.12	9.96	12.27	0.75	9.20	92.41	12.12	91
						Average	**92.88**		**90.10**

9.6 No-Load Input Power

No load input power soak time: 15 mins.

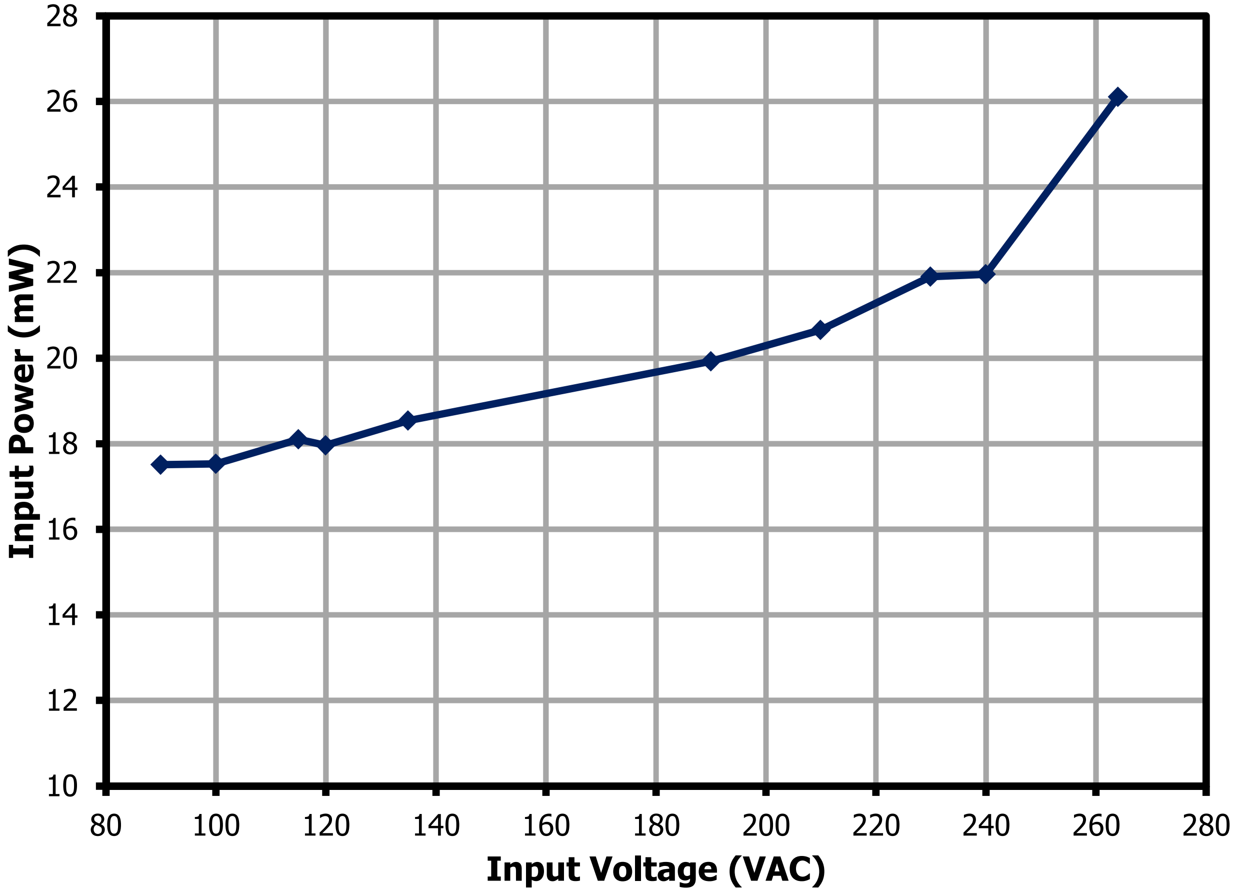


Figure 10 – Input Power vs. Input Line Voltage at No-Load, Room Temperature.

9.7 Line and Load Regulation

9.7.1 Line Regulation at Full Load (at PCB)

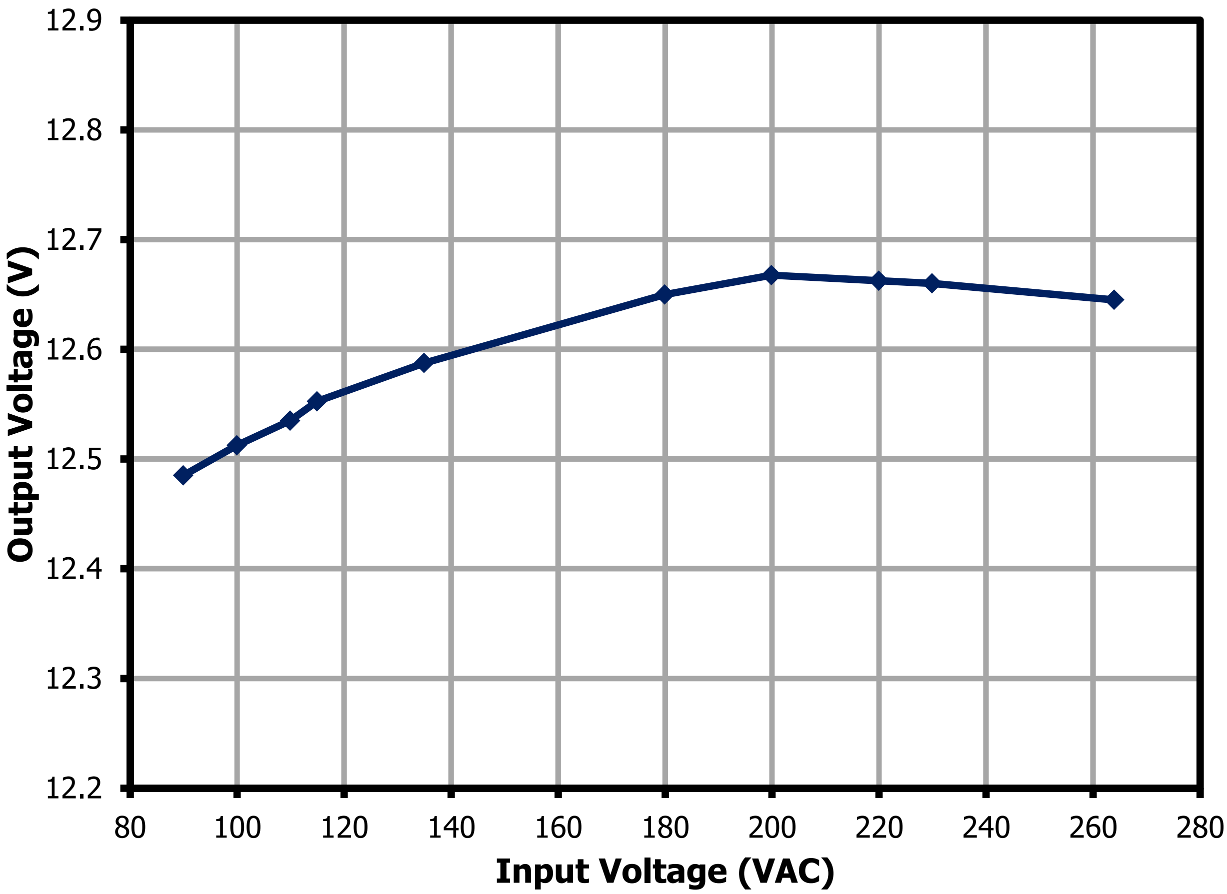


Figure 11 – Measured at PCB, Room Temperature.

9.7.2 Load Regulation

9.7.2.1 At PCB

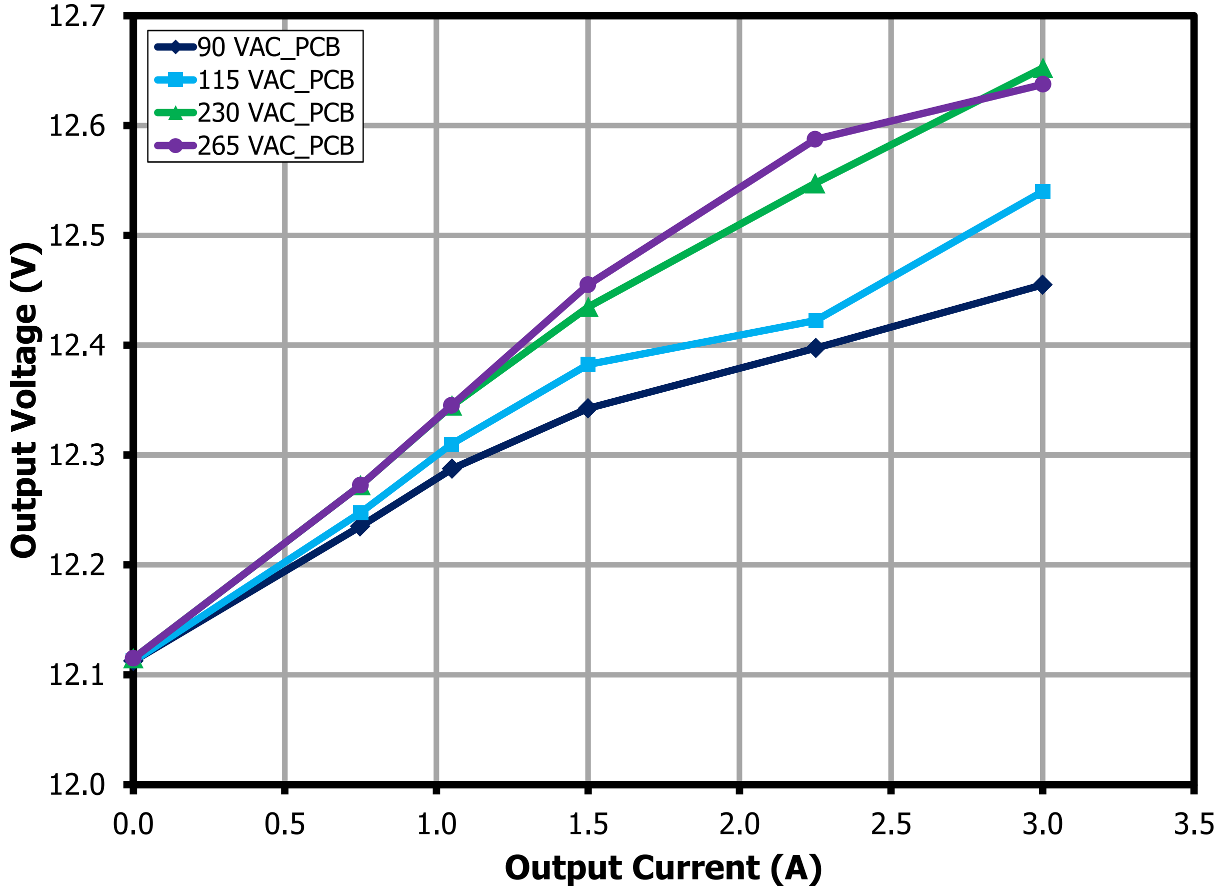


Figure 12 – Measured at PCB, Room Temperature.

9.7.2.2 At End of Cable (1.8 M, #22 AWG)

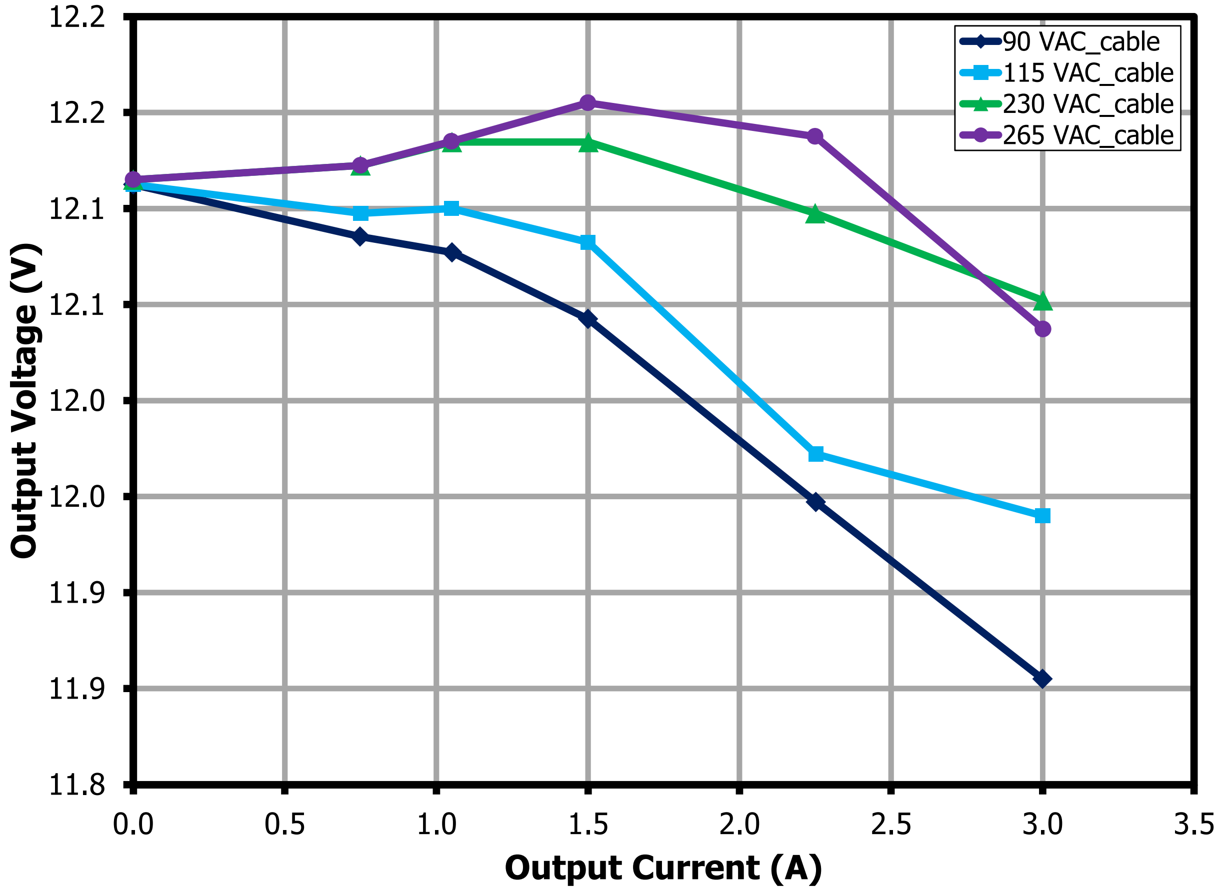


Figure 13 – Measured at PCB and at End of Cable, Room Temperature.

10 Waveforms

10.1 Output Voltage Ripple

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one 10 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

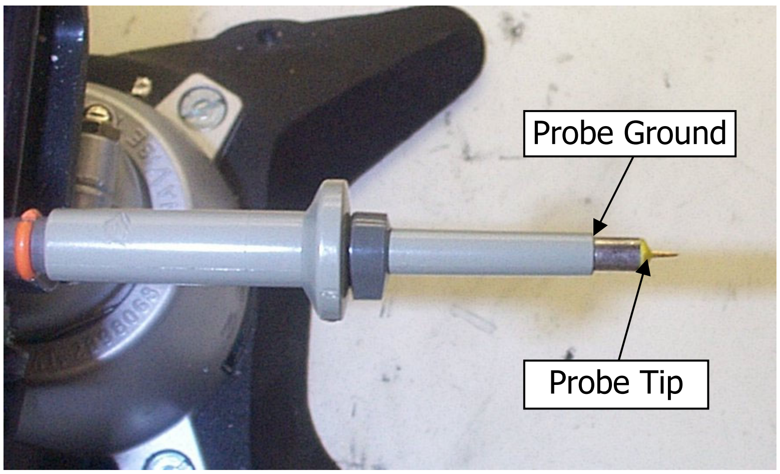


Figure 14 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

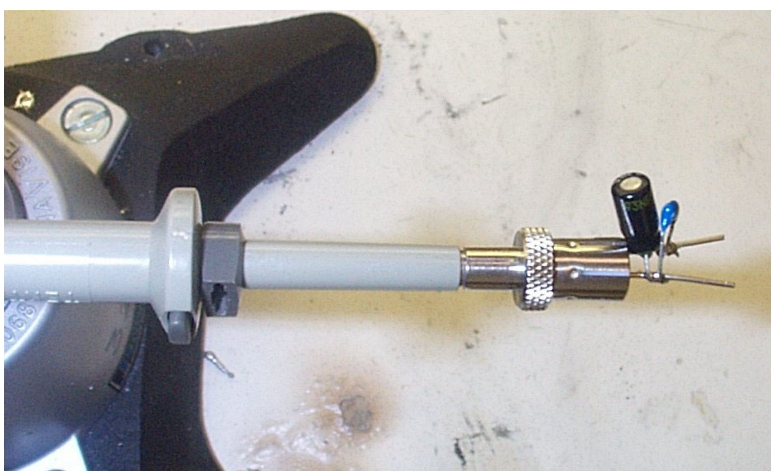


Figure 15 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

10.2 Measurement Results

10.2.1 Output Ripple Voltage Graph from 0% - 100%

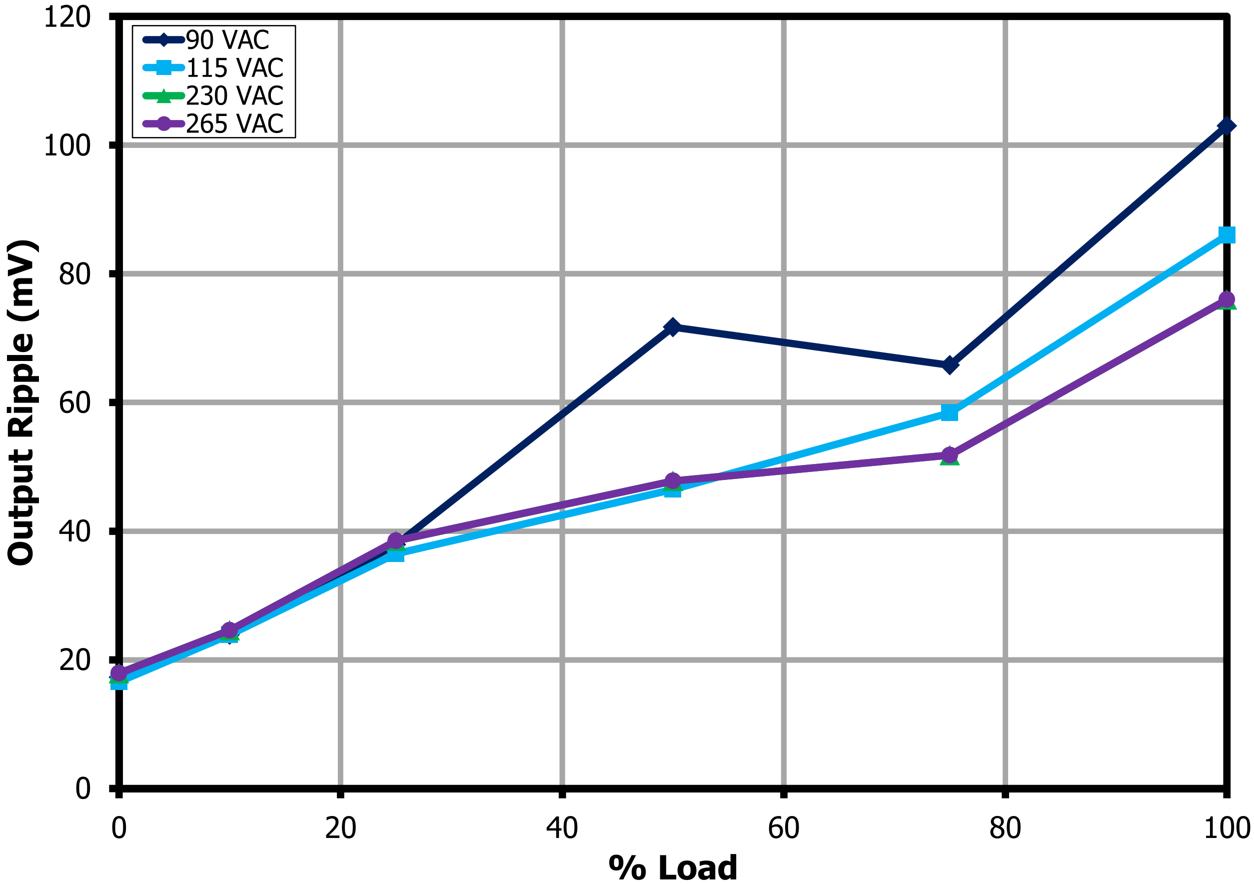


Figure 16 – Measured at the End of Cable at Room Temperature.

10.2.2 Output Ripple Voltage Waveforms for 12 V Output

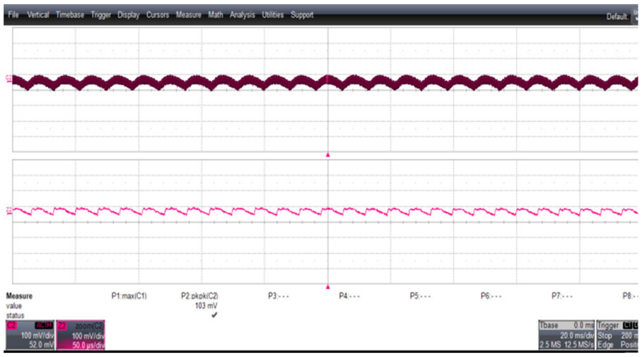


Figure 17 – 90 VAC Input.
Condition: 12 V – 3 A
V_{RIPPLE}, 100 mV / div., 20 ms / div.
Zoom, 50 μs / div.
$V_{RIPPLE(PK-PK)}$: 103 mV.

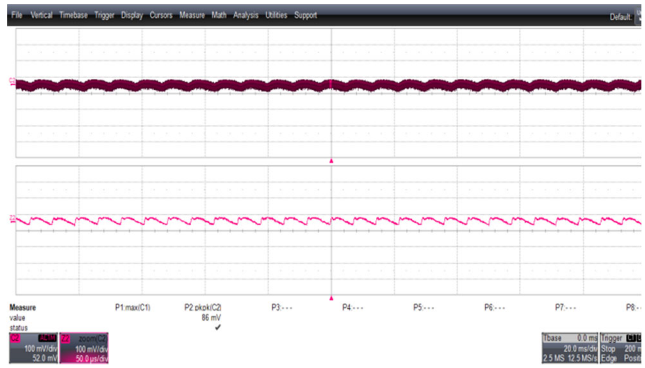


Figure 18 – 115 VAC Input.
Condition: 12 V – 3 A.
V_{RIPPLE}, 100 mV / div., 20 ms / div.
Zoom, 50 μs / div.
$V_{RIPPLE(PK-PK)}$: 86 mV.

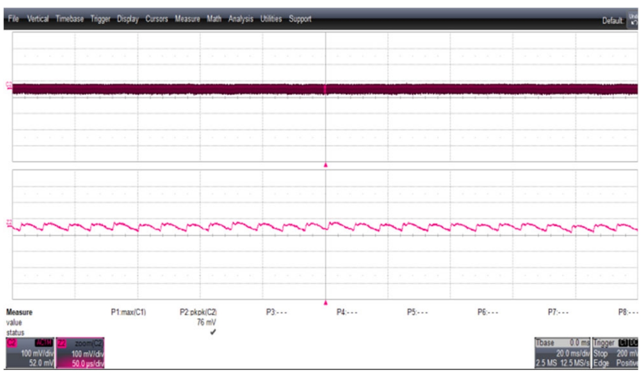


Figure 19 – 230 VAC Input.
Condition: 12 V – 3 A.
V_{RIPPLE}, 100 mV / div., 20 ms / div.
Zoom, 50 μs / div.
$V_{RIPPLE(PK-PK)}$: 76 mV.

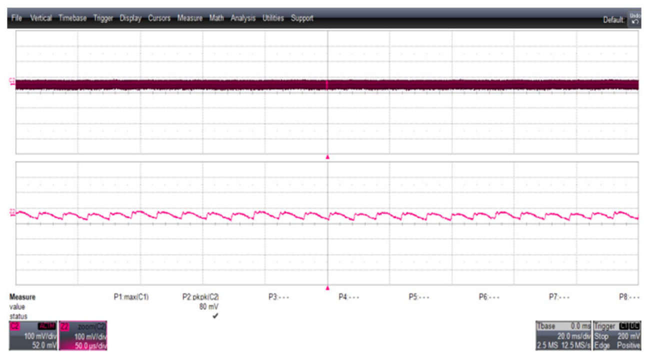


Figure 20 – 265 VAC Input.
Condition: 12 V – 3 A.
V_{RIPPLE}, 100 mV / div., 20 ms / div.
Zoom, 50 μs / div.
$V_{RIPPLE(PK-PK)}$: 80 mV.

10.3 Start-up Performance

Measured at the end of the cable using electronic load having a slew rate of 200 mA/S.

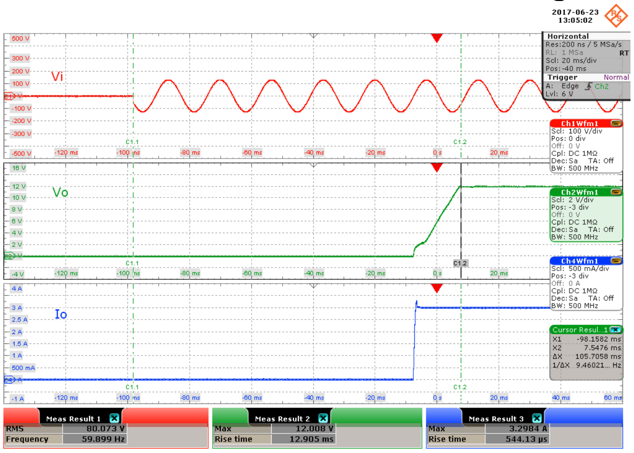


Figure 21 – 90 VAC Input.
Upper: V_{IN}, 100 V / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 500 mA / div., 20 ms / div.
Start-up Time: 105.7058 ms.

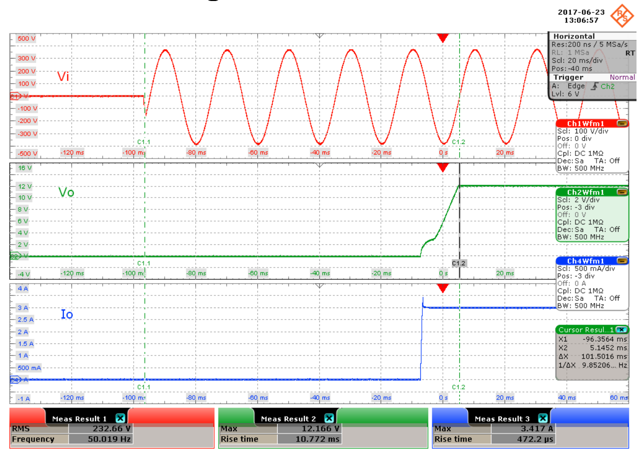


Figure 22 – 265 VAC Input.
Upper: V_{IN}, 100 V / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 500 mA / div., 20 ms / div.
Start-up Time: 101.5016 ms.

10.4 Output Load Transient

Measured at the end of the cable with a slew rate of 800 mA/S

10.4.1 Dynamic Loading from 0% - 100%

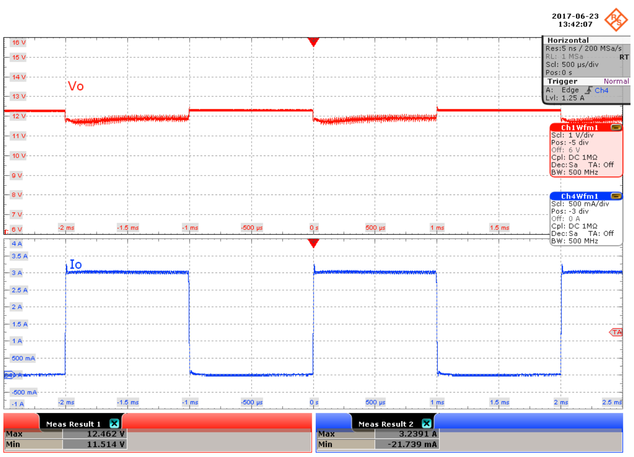


Figure 23 – 90 VAC Input.
Upper: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 500 mA / div., 500 µs / div.
V_{MAX}: 12.462 V.
V_{MIN}: 11.514 V.

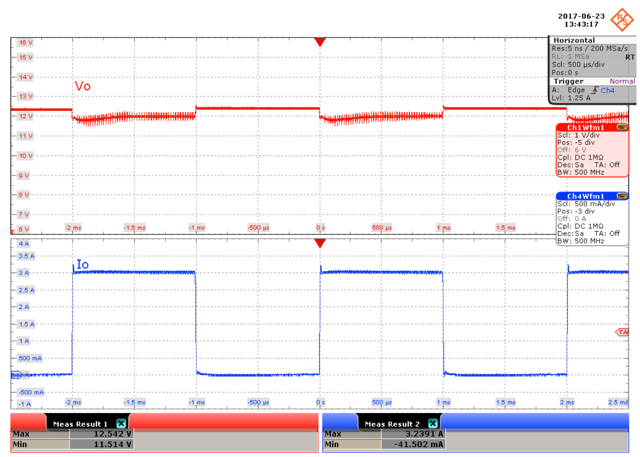


Figure 24 – 265 VAC Input.
Upper: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 500 mA / div., 500 µs / div.
V_{MAX}: 12.542 V.
V_{MIN}: 11.514 V.

10.4.2 Dynamic Loading from 50% - 100%

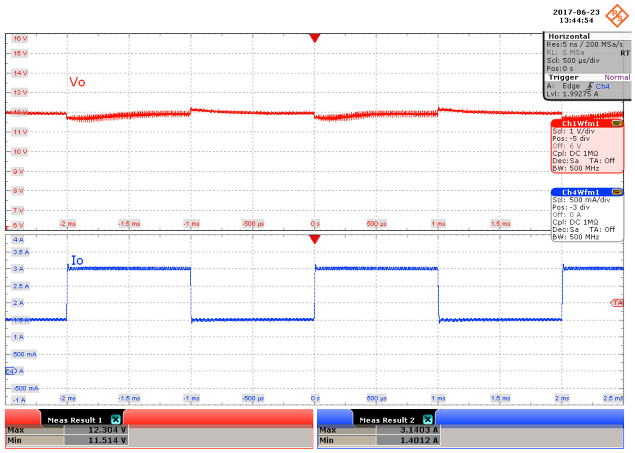


Figure 25 – 90 VAC Input.
Upper: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 500 mA / div., 500 µs / div.
V_{MAX}: 12.304 V.
V_{MIN}: 11.514 V.

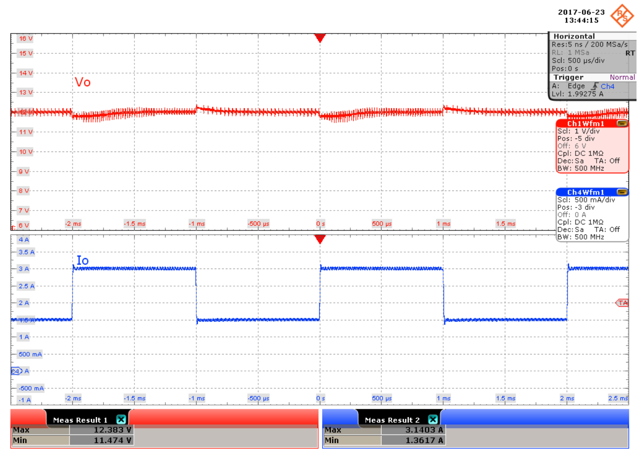


Figure 26 – 265 VAC Input.
Upper: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 500 mA / div., 500 µs / div.
V_{MAX}: 12.383 V.
V_{MIN}: 11.474 V.

10.5 Drain Voltage and Current Waveforms

10.5.1 Start-up Operation V_{DS} and I_{DS}

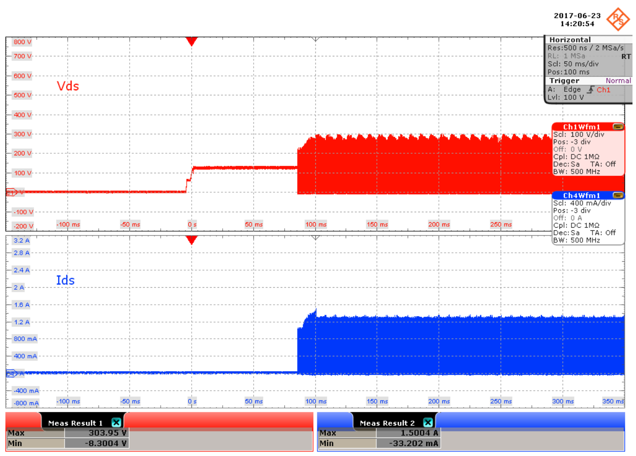


Figure 27 – 90 VAC Input.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 400 mA / div., 50 ms / div.
$V_{DS(MAX)}$: 303.95 V.
$I_{DS(MAX)}$: 1.5004 A.

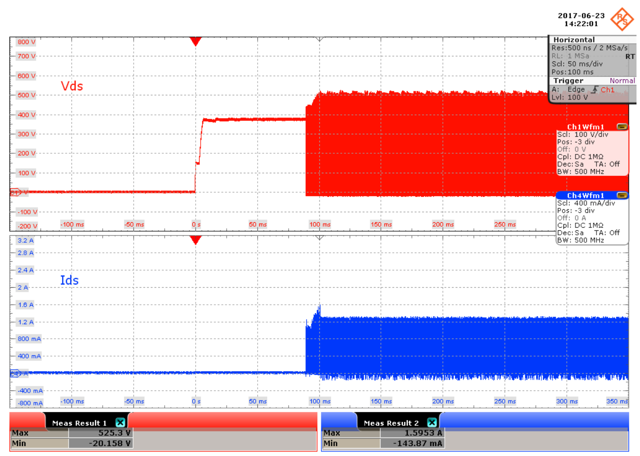


Figure 28 – 265 VAC Input.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 400 mA / div., 50 ms / div.
$V_{DS(MAX)}$: 525.30 V.
$I_{DS(MAX)}$: 1.5953 A.

10.5.2 Normal Operation V_{DS} and I_{DS}

10.5.2.1 100% Load

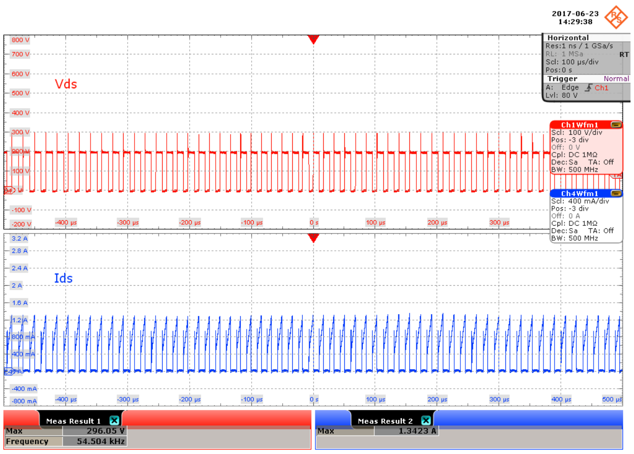


Figure 29 – 90 VAC Input.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 400 mA / div., 100 μs / div.

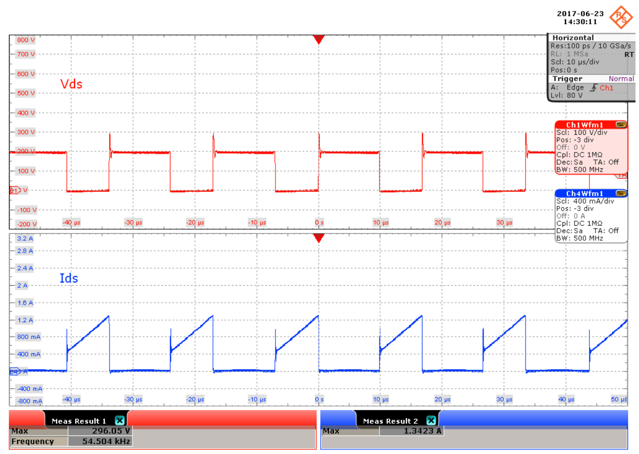


Figure 30 – 90 VAC Input.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 400 mA / div., 10 μs / div.
$V_{DS(MAX)}$: 296.05 V.
$I_{DS(MAX)}$: 1.3423 A.

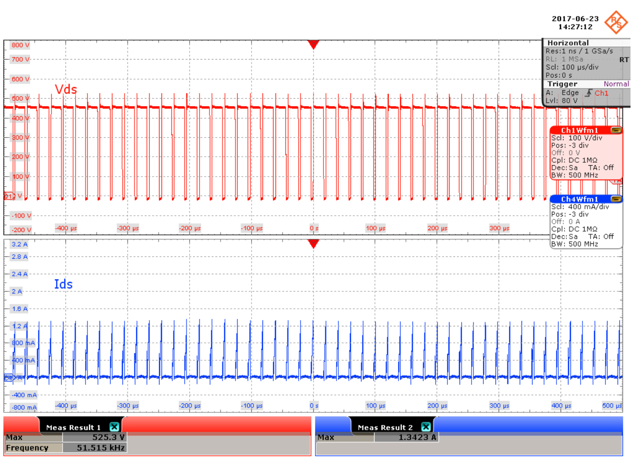


Figure 31 – 265 VAC Input.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 400 mA / div., 100 μs / div.

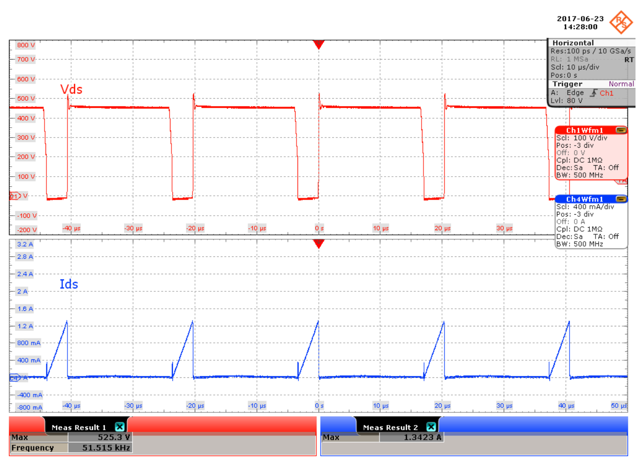


Figure 32 – 265 VAC Input.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 400 mA / div., 10 μs / div.
$V_{DS(MAX)}$: 525.30 V.
$I_{DS(MAX)}$: 1.3423 A.

10.5.3 Normal Operation SyncRec FET V_{DS} and I_{DS}

10.5.3.1 100% Load

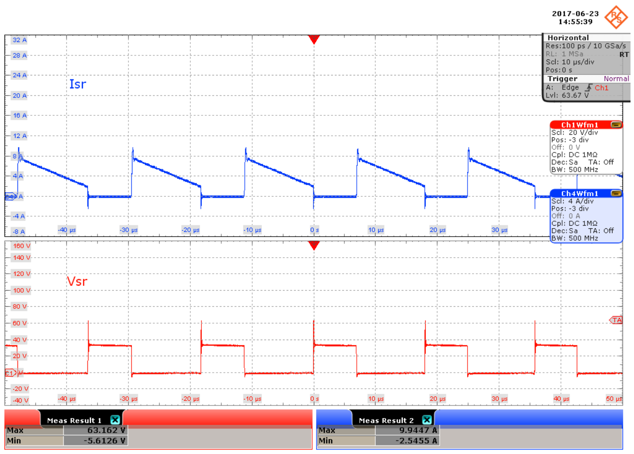


Figure 33 – 90 VAC Input.
Upper: I_{SR}, 4 A / div.
Lower: V_{SR}, 20 V / div., 10 μs / div.
$V_{SR(MAX)}$: 63.162 V.
$I_{DS(MAX)}$: 9.9447 A.

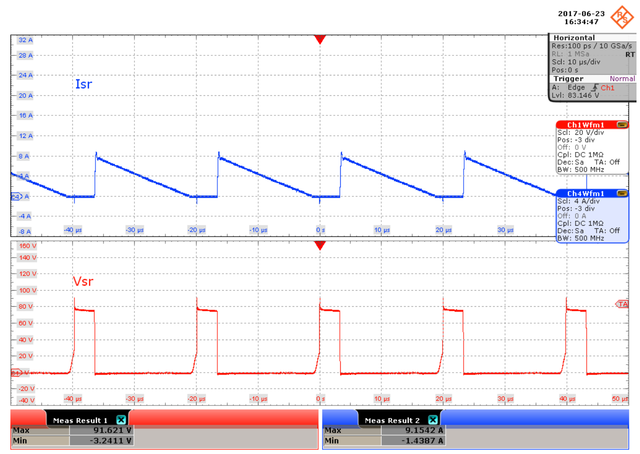


Figure 34 – 265 VAC Input.
Upper: I_{SR}, 4 A / div.
Lower: V_{SR}, 20 V / div., 10 μs / div.
$V_{SR(MAX)}$: 91.621 V.
$I_{SR(MAX)}$: 9.1542 A.

10.6 Output Short Waveforms

Short the main output (12 V) and monitor I_{DS}, output voltage and output current.

Fault during start-up

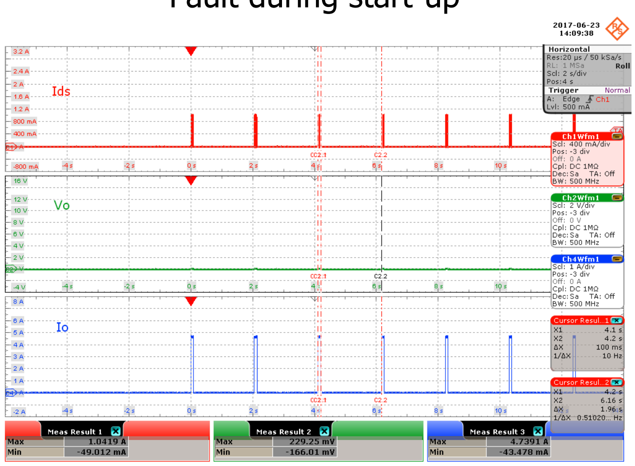


Figure 35 – 90 VAC Input.
Condition: 12 V – Shorted.
Upper: I_{DS}, 400 mA / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A / div., 2 s / div.
$T_{ON(AR)}$: 100 ms.
$T_{OFF(AR)}$: 1.96 s.

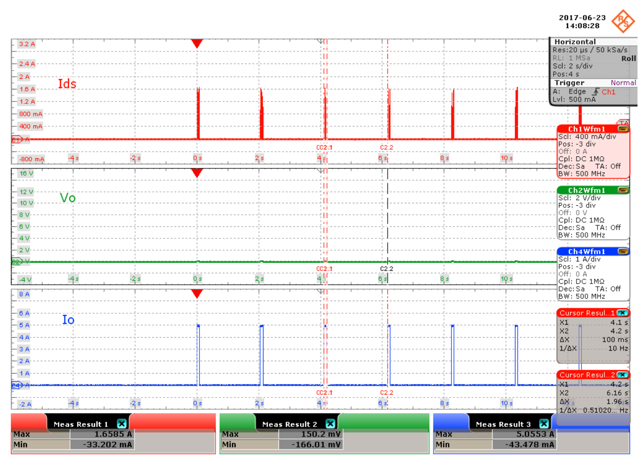


Figure 36 – 265 VAC Input.
Condition: 12 V – Shorted.
Upper: I_{DS}, 400 mA / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A / div., 2 s / div.
$T_{ON(AR)}$: 100 ms.
$T_{OFF(AR)}$: 1.96 s.

10.7 Fault During Normal Operation

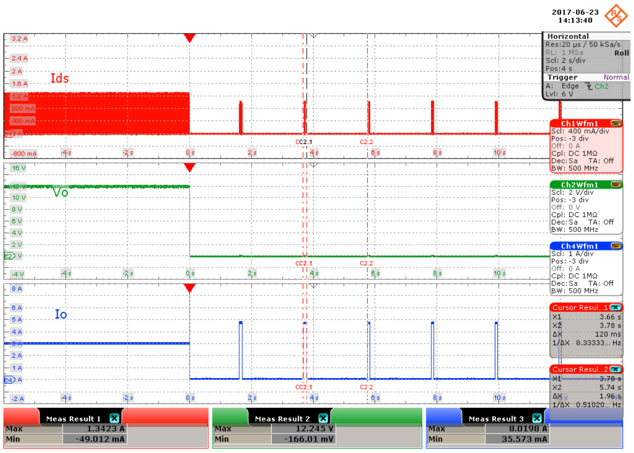


Figure 37 – 90 VAC Input.
Condition: 12 V – Shorted.
Upper: I_{DS}, 400 mA / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A / div., 2 s / div.
$T_{ON(AR)}$: 120 ms.
$T_{OFF(AR)}$: 1.96 s.

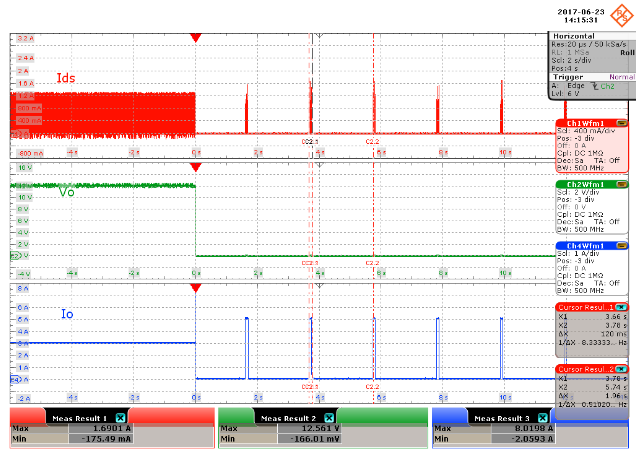


Figure 38 – 265 VAC Input.
Condition: 12 V – Shorted.
Upper: I_{DS}, 400 mA / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A / div., 2 s / div.
$T_{ON(AR)}$: 120 ms.
$T_{OFF(AR)}$: 1.96 s.

10.8 Output Voltage and Current Waveforms During Feedback Open

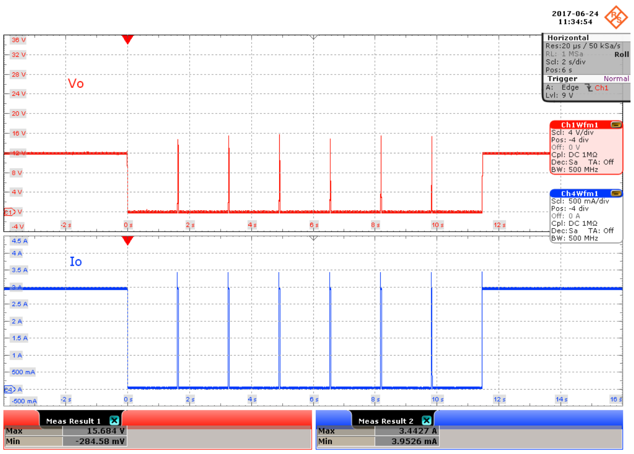


Figure 39 – 90 VAC Input.
Condition: R8 – Open.
Upper: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 500 mA / div.
$V_{OVP(MAX)}$: 15.684 V.

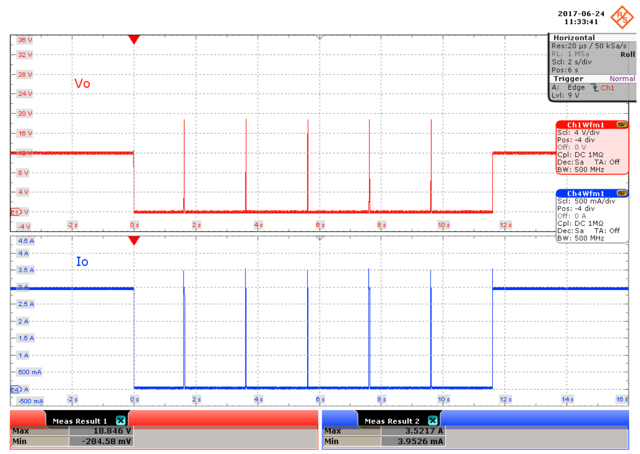


Figure 40 – 265 VAC Input.
Condition: R8 – Open.
Upper: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 500 mA / div., 2 s / div.
$V_{OVP(MAX)}$: 18.846 V.

10.9 Brown-In and Brown-Out

Set brown-in / brown-out profile to 6 V / min all the way to 0 starting from 90 VAC.

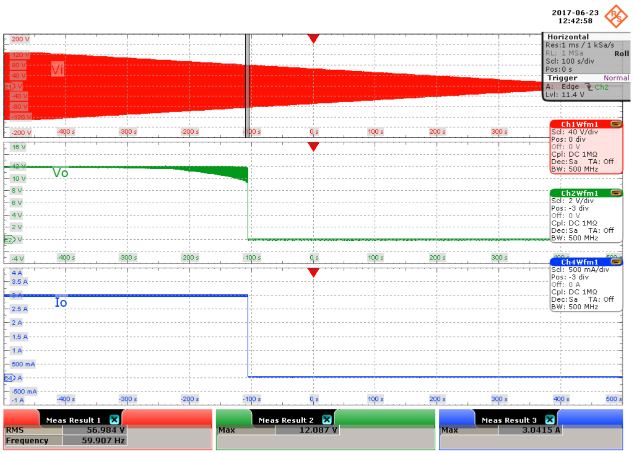


Figure 41 – 90 VAC Input.
Condition: 12 V – 3 A.
Upper: V_{IN}, 40 V / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 500 mA / div., 100 s / div.
Brown-Out: 56.984 VAC.

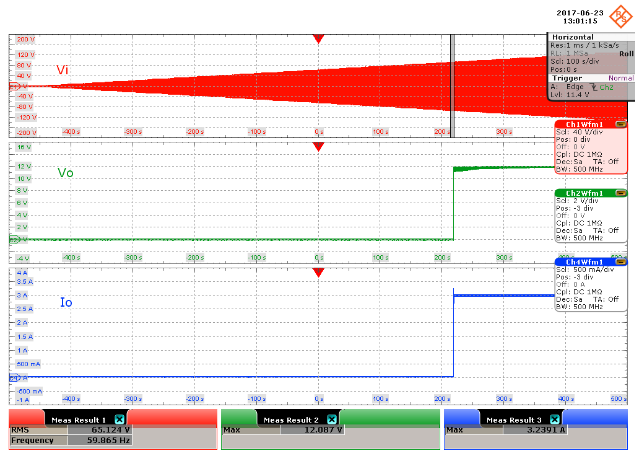


Figure 42 – 90 VAC Input.
Condition: 12 V – 3 A.
Upper: V_{IN}, 40 V / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 500 mA / div., 100 s / div.
Brown-In: 65.124 VAC.

10.10 Line Undervoltage and Overvoltage Protection

10.10.1 Line UV+ and UV-

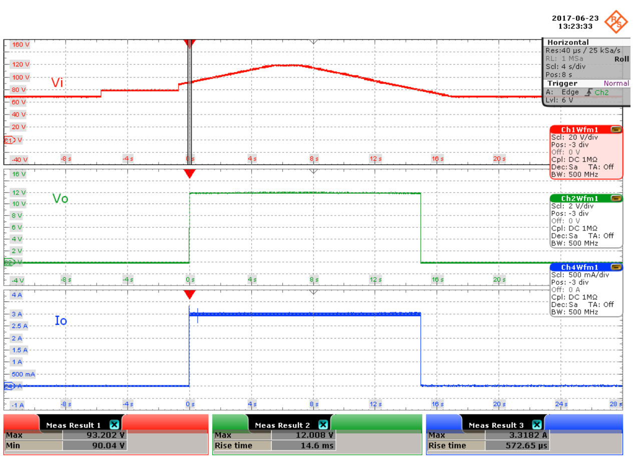


Figure 43 – 70 VDC Input.
Condition: 12 V – 3 A.
Upper: V_{IN}, 20 V / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 500 mA / div., 4 s / div.
Line UV+: 93.202 VDC.

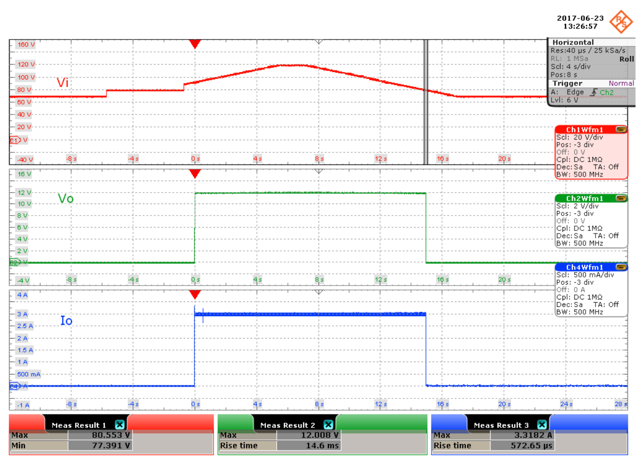


Figure 44 – 70 VDC Input.
Condition: 12 V – 3 A.
Upper: V_{IN}, 20 V / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 500 mA / div., 4 s / div.
Line UV-: 80.553 VDC.

10.10.2 Line OV+ and OV-

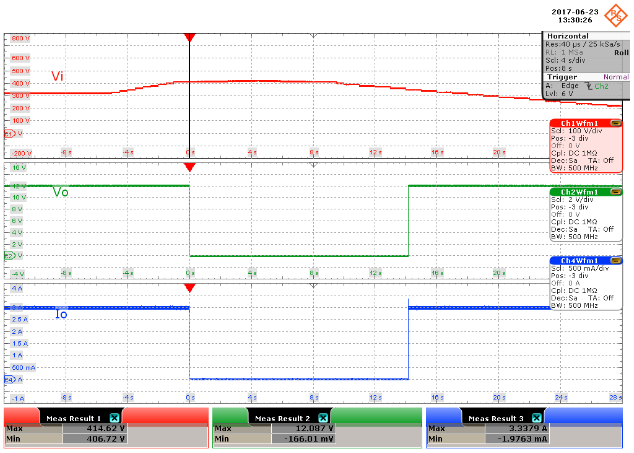


Figure 45 – 320 VDC Input.
Condition: 12 V – 3 A.
Upper: V_{IN}, 100 V / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 500 mA / div., 4 s / div.
Line OV+: 414.62 VDC.

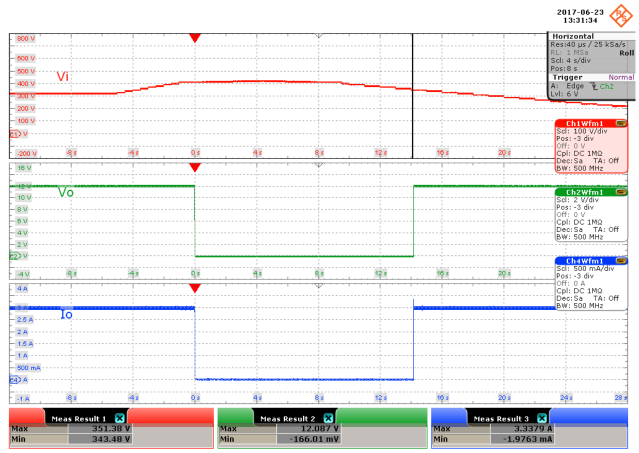


Figure 46 – 320 VDC Input.
Condition: 12 V – 3 A.
Upper: V_{IN}, 100 V / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 500 mA / div., 4 s / div.
Line OV-: 351.38 VDC.

10.11 Thermal Performance

10.11.1 Thermal Performance at 90 VAC

Ambient temperature is 28.5 ºC

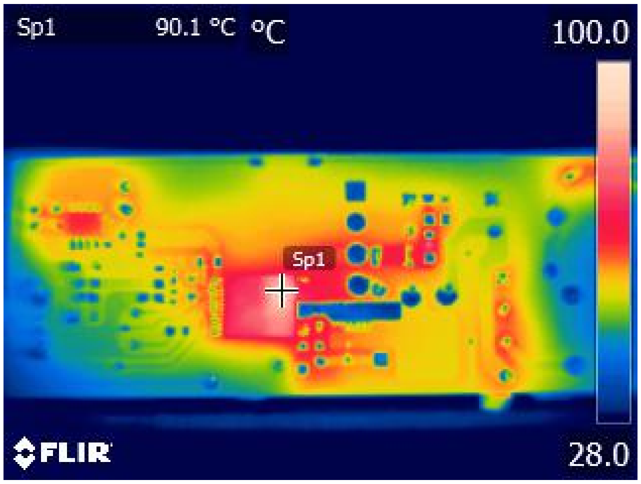


Figure 47 – U1 – INN3166C Controller.
Spot: 90.1 ºC.

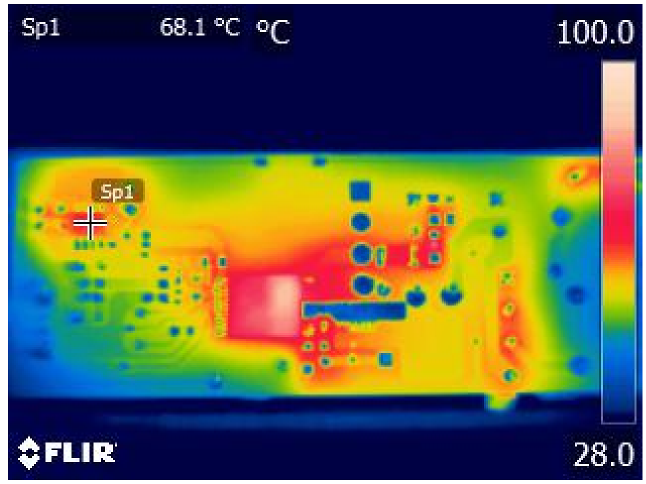


Figure 48 – Q1 – SR FET.
Spot: 68.1 ºC.

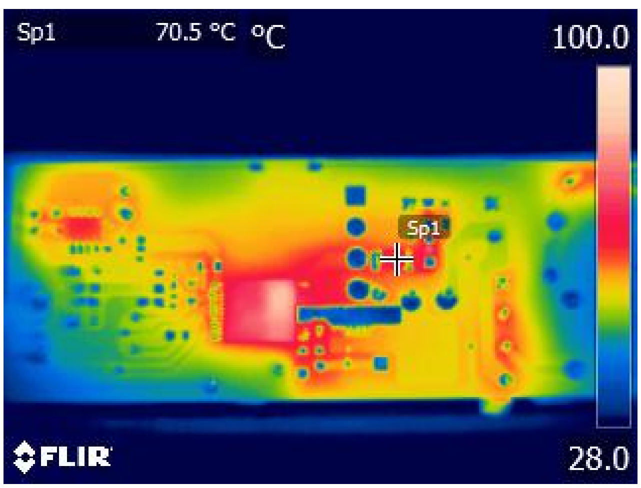


Figure 49 – D1 – Primary Snubber Diode.
Spot: 70.5 ºC.

Figure 50 – T1 – Transformer (Top Side).
Spot: 70.5 ºC.

Figure 51 – BR1 – Bridge Rectifier Diode.
Spot: 71.9 ºC.

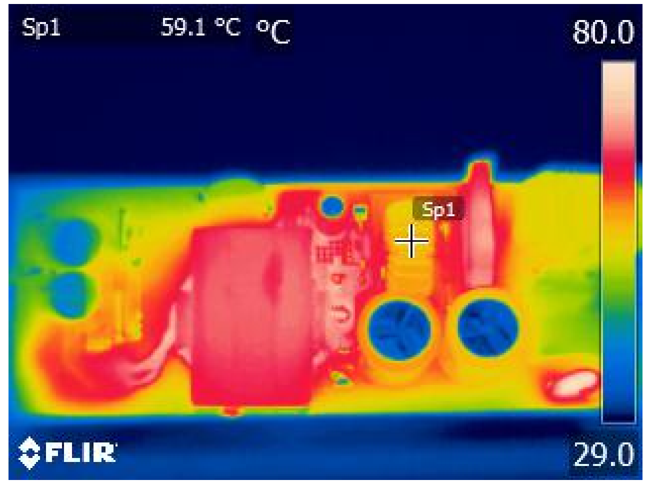


Figure 52 – L2 – Differential Choke.
Spot: 59.1 ºC.

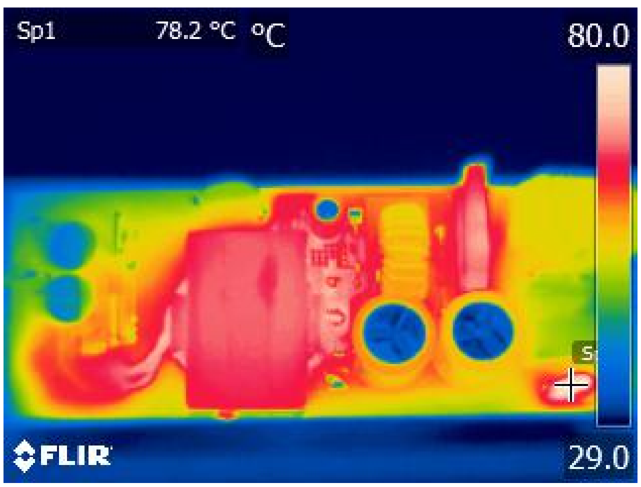


Figure 53 – RT1 – Thermistor.
Spot: 78.2 ºC.

Figure 54 – R1 – Line Voltage Sense Resistor.
Spot: 67.9 ºC.

10.11.2 Thermal Performance at 265 VAC

Ambient temperature is 28.5 ºC

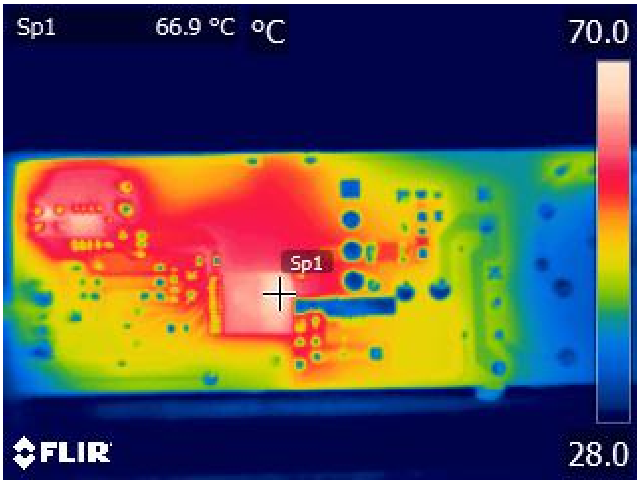


Figure 55 – U1 – INN3166C Controller.
Spot: 66.9 ºC.

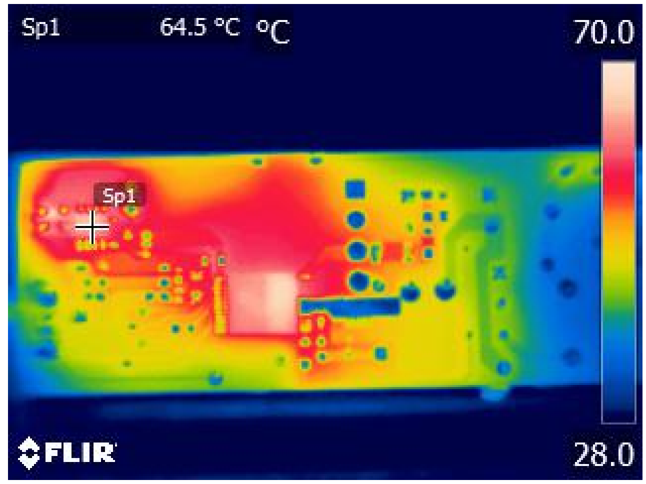


Figure 56 – Q1 – SR FET.
Spot: 64.5 ºC.

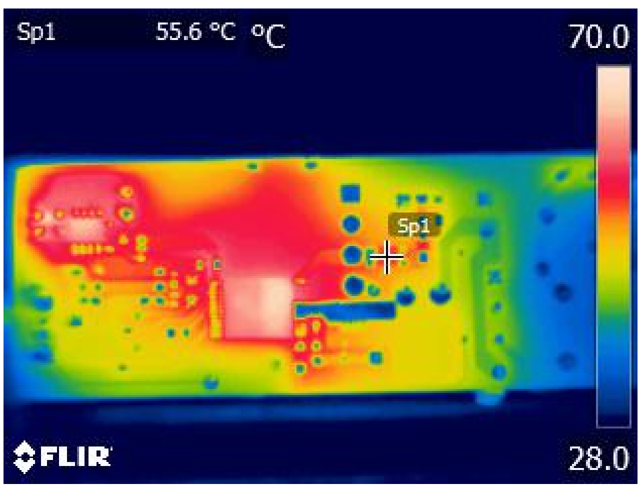


Figure 57 – D1 – Primary Snubber Diode.
Spot: 55.6 ºC.

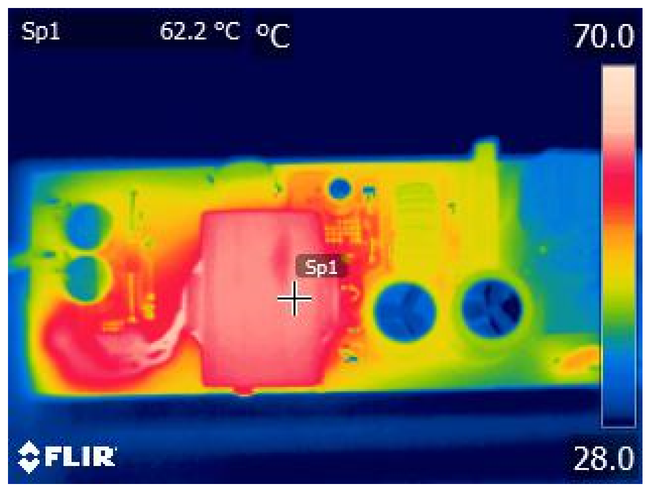


Figure 58 – T1 – Transformer (Top Side).
Spot: 62.2 ºC.

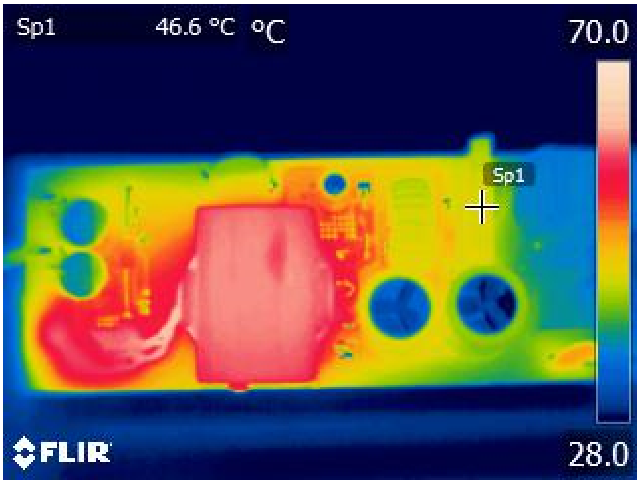


Figure 59 – BR1 – Bridge Rectifier Diode.
Spot: 46.6 ºC.

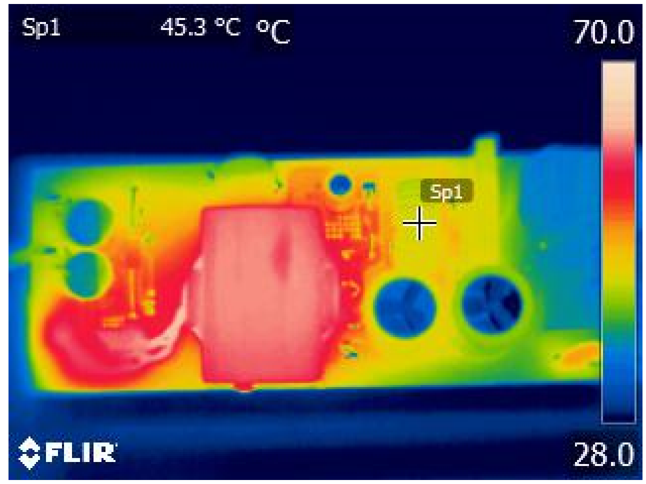


Figure 60 – L2 – Differential Choke.
Spot: 45.3 ºC.

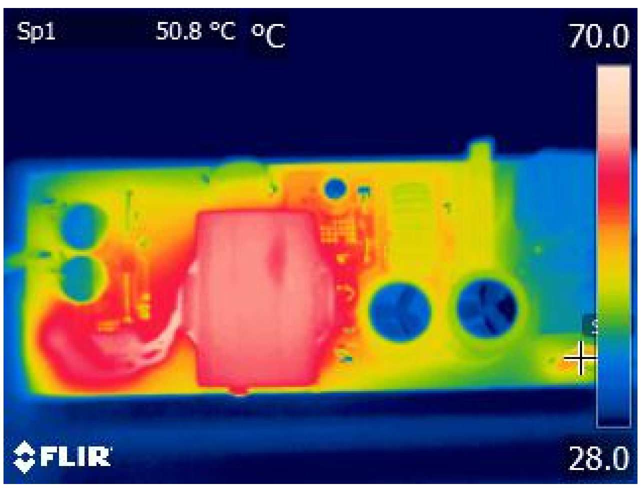


Figure 61 – RT1 – Thermistor.
Spot: 50.8 ºC.

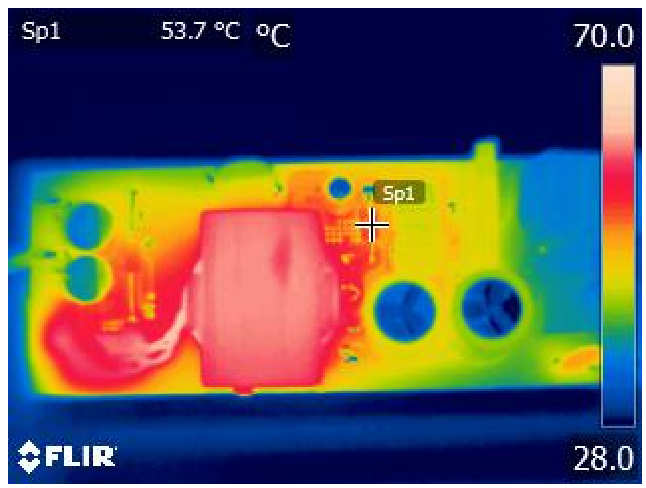


Figure 62 – R1 – Line Voltage Sense Resistor.
Spot: 53.7 ºC.

10.11.3 Thermal Performance at 45 ºC

Place the test unit inside an acrylic box. Increase chamber temperature to 45 ºC. Soak time of 2 hrs. Monitor all components and ambient temperature.

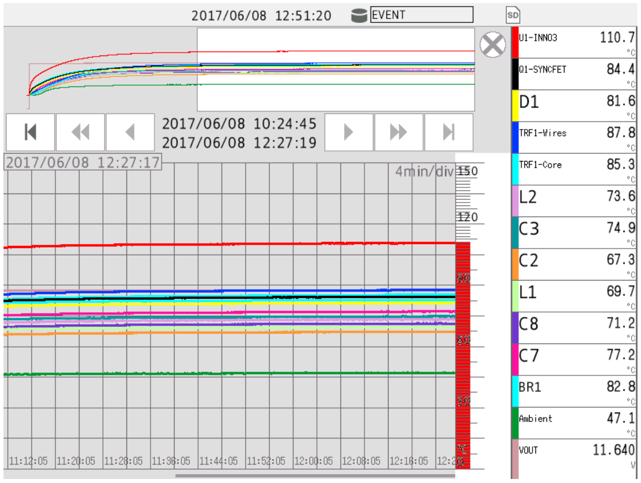


Figure 63 – 90 VAC Input.
U1 – INN3166C Controller.
Temp: 110.7 ºC.

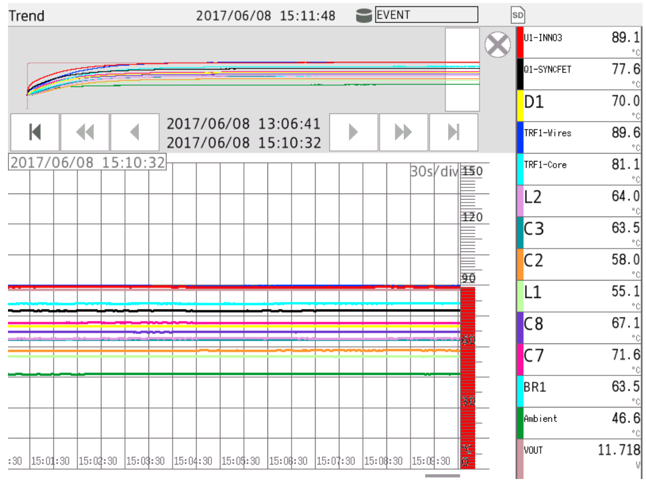


Figure 64 – 265 VAC Input.
U1 – INN3166C Controller.
Temp: 89.1 ºC.

10.12 Thermal Shutdown and Recovery

10.12.1 Shutdown Temperature at 90 VAC and 265 VAC

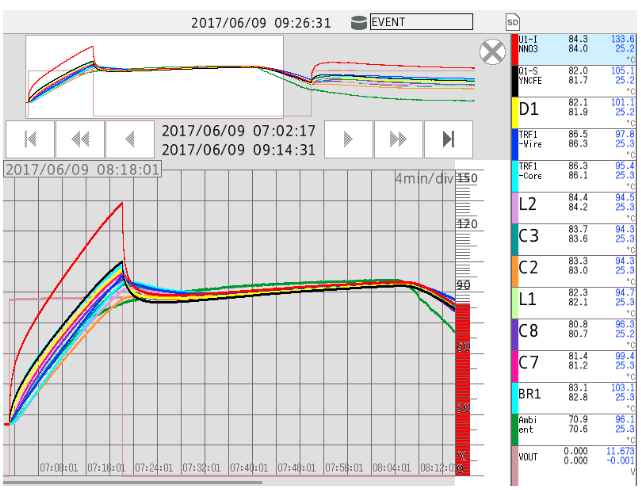


Figure 65 – 90 VAC Input.
U1 – INN3166C Controller.
Temp: 133.6 ºC.

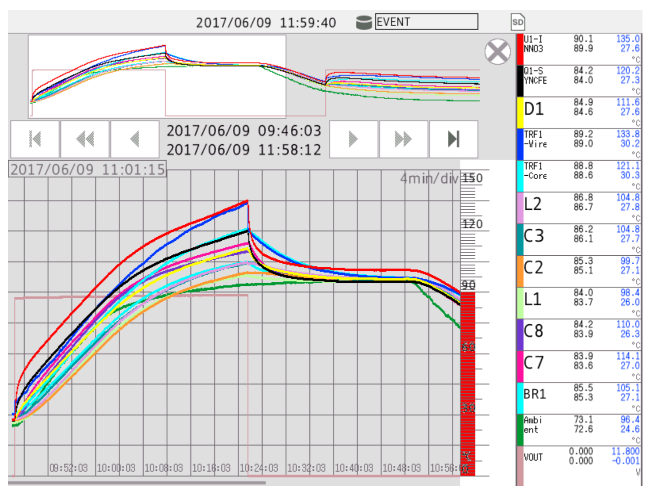


Figure 66 – 265 VAC Input.
U1 – INN3166C Controller.
Temp: 135.0 ºC.

10.12.2 Recovery Temperature at 90 VAC and 265 VAC

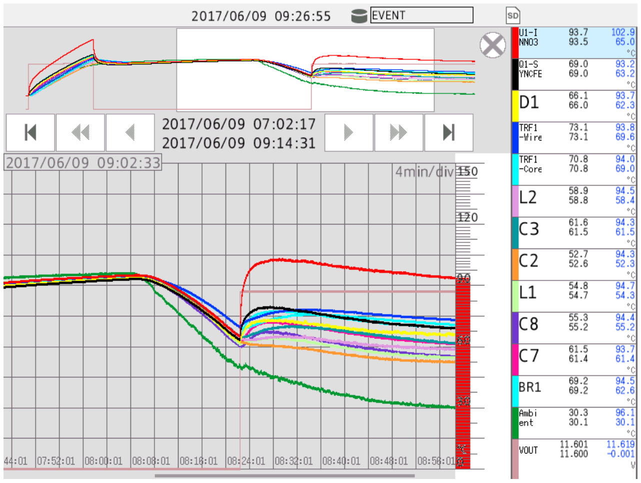


Figure 67 – 90 VAC Input.
U1 – INN3166C Controller.
Temp: 65.0 ºC.

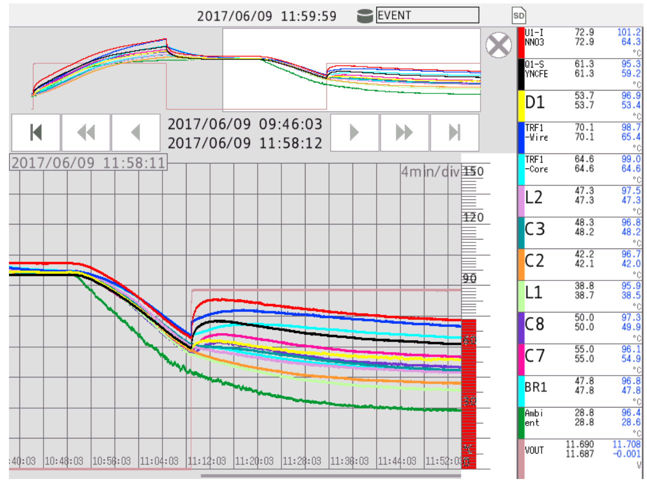


Figure 68 – 265 VAC Input.
U1 – INN3166C Controller.
Temp: 64.3 ºC.

11 Conducted EMI

11.1 Test Setup Equipment

11.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power Hi-tester.
4. Chroma measurement test fixture.
5. 4 Ω resistor load.
6. Input voltage set at 115 VAC and 230 VAC.

11.2 Test Set-up

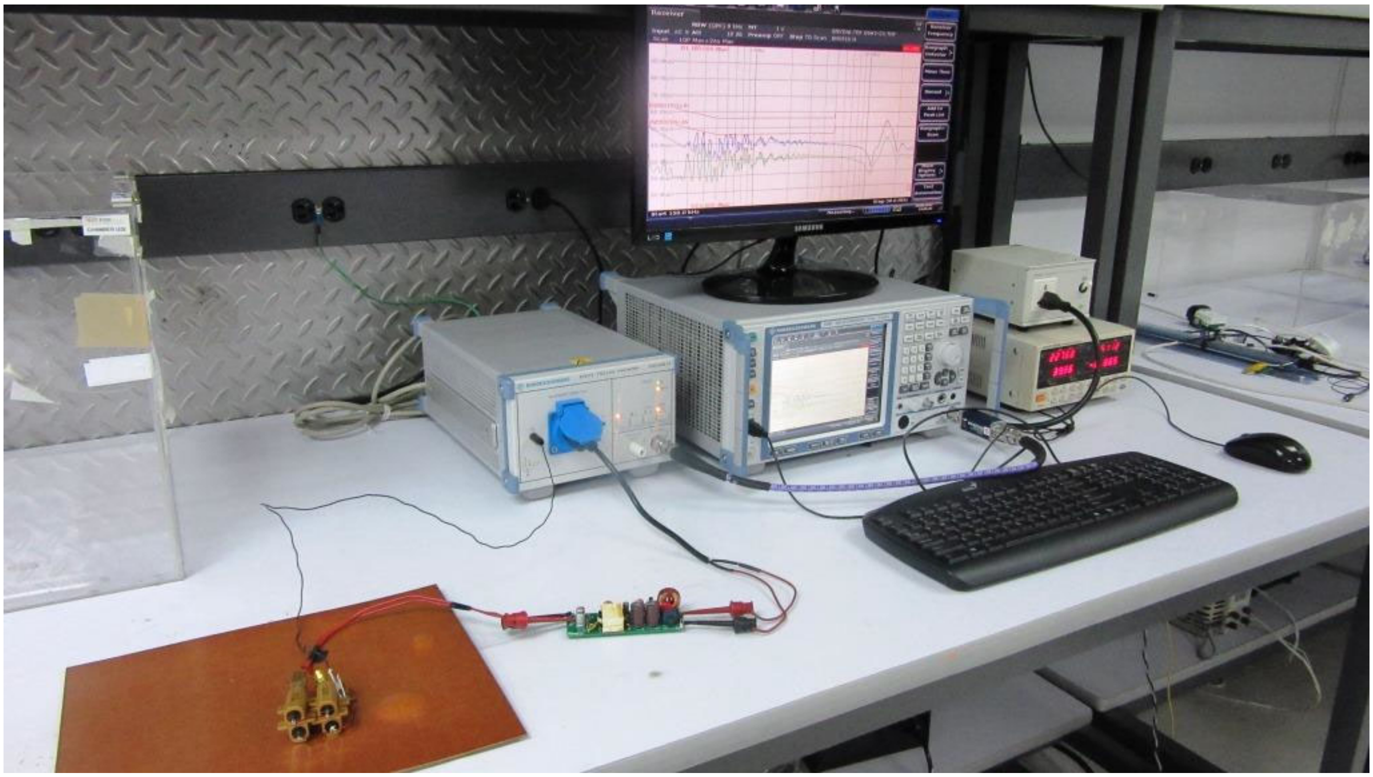
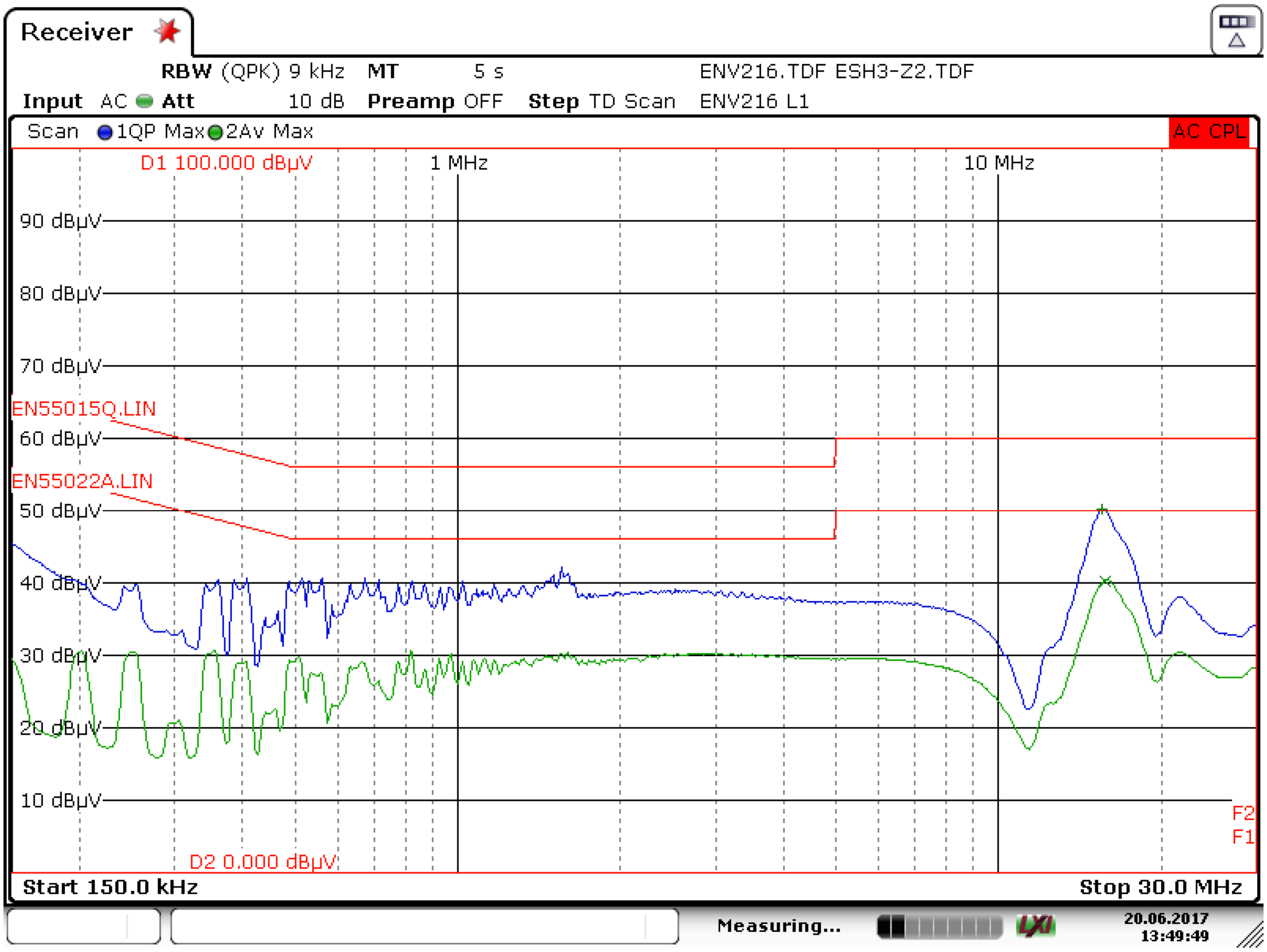


Figure 69 – Test Set-up.

11.3 Conductive EMI with Earth Grounded Output (QP / AV)

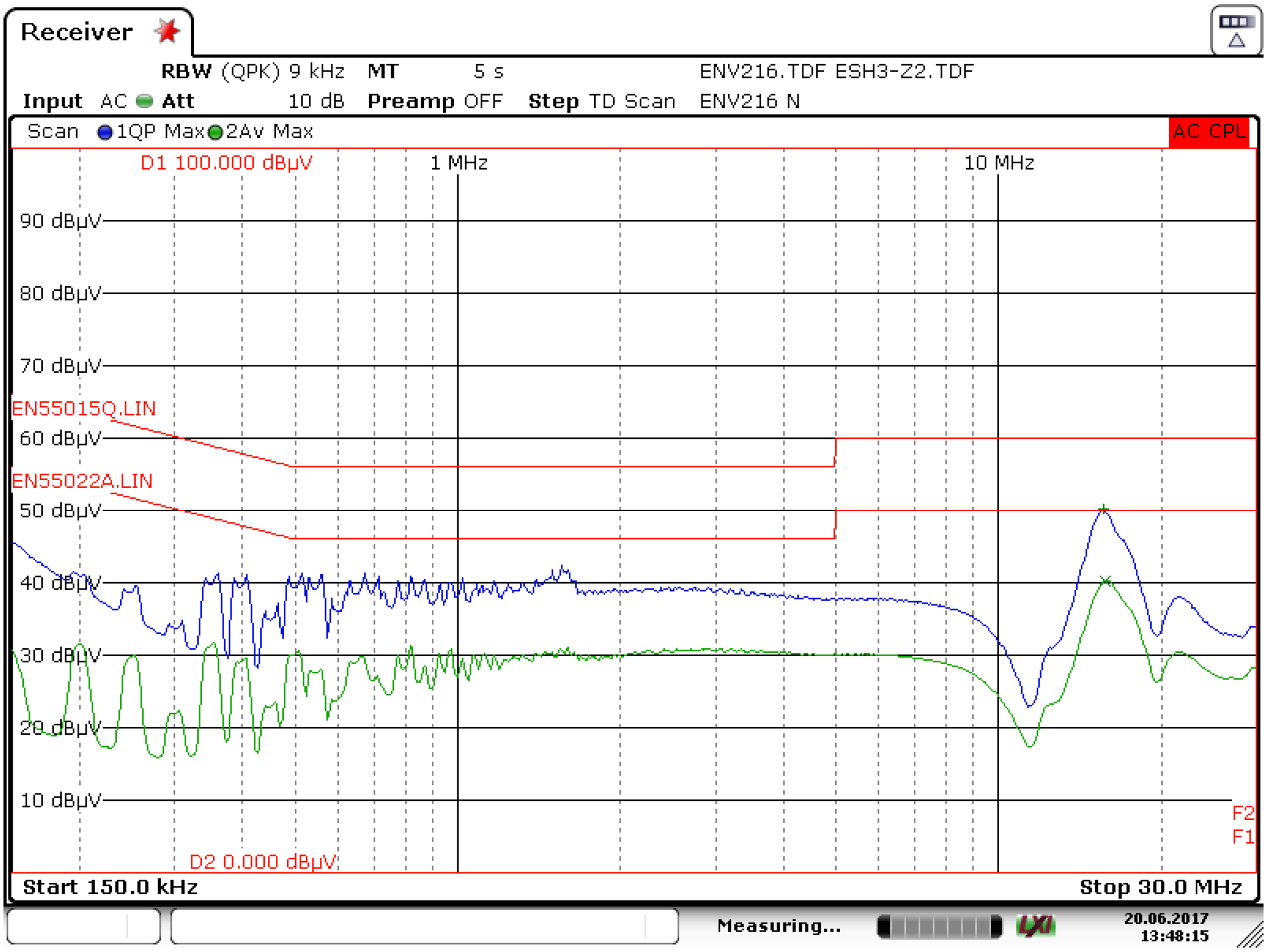
11.3.1 115 VAC Line



Date: 20.JUN.2017 13:49:49

Figure 70 – PE Connected to the Negative Output, Line.

11.3.2 115 VAC Neutral



Date: 20.JUN.2017 13:48:15

Figure 71 – PE Connected to the Negative Output, Neutral.

11.3.3 230 VAC Line

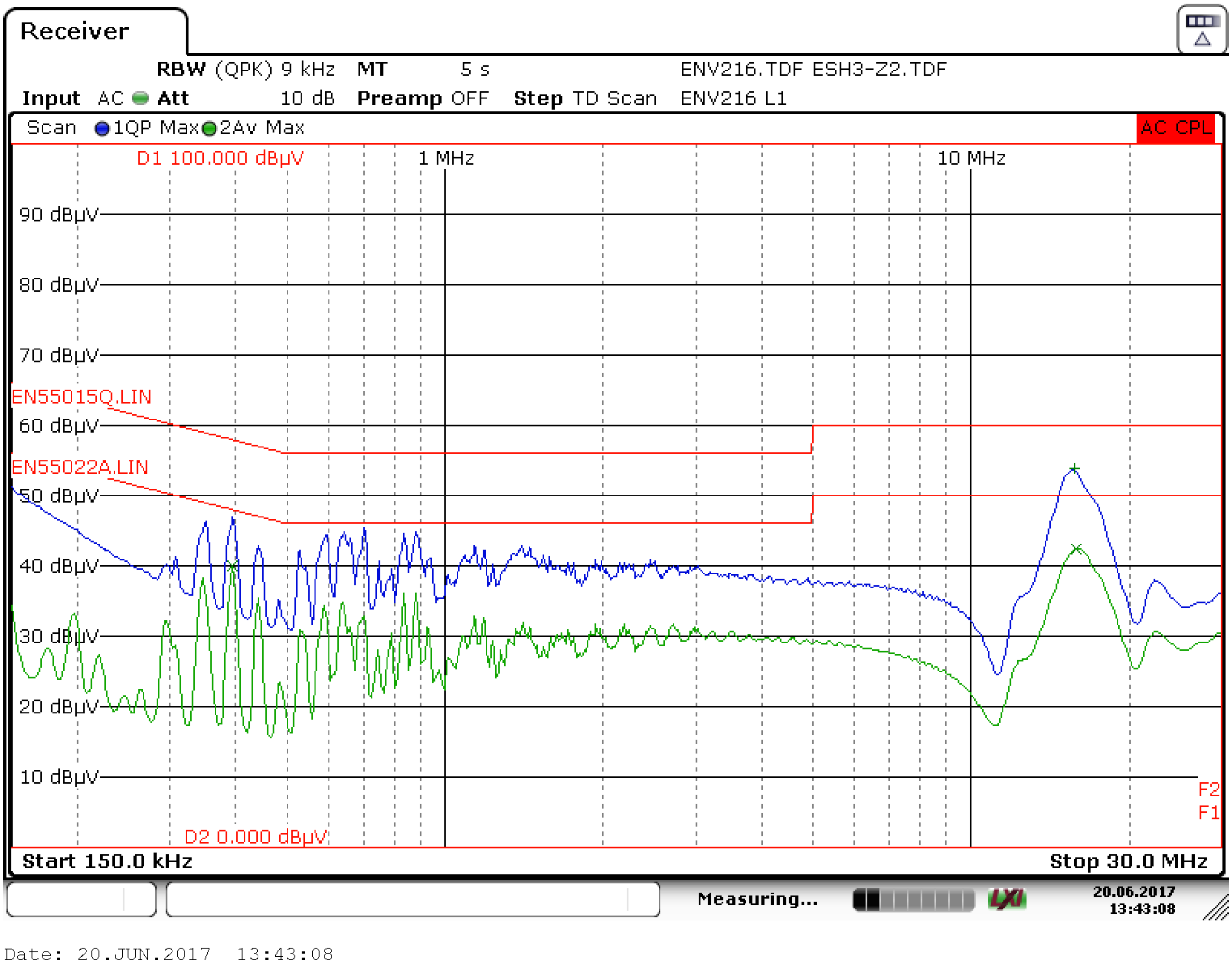


Figure 72 – PE Connected to the Negative Output, Line.

11.3.4 230 VAC Neutral

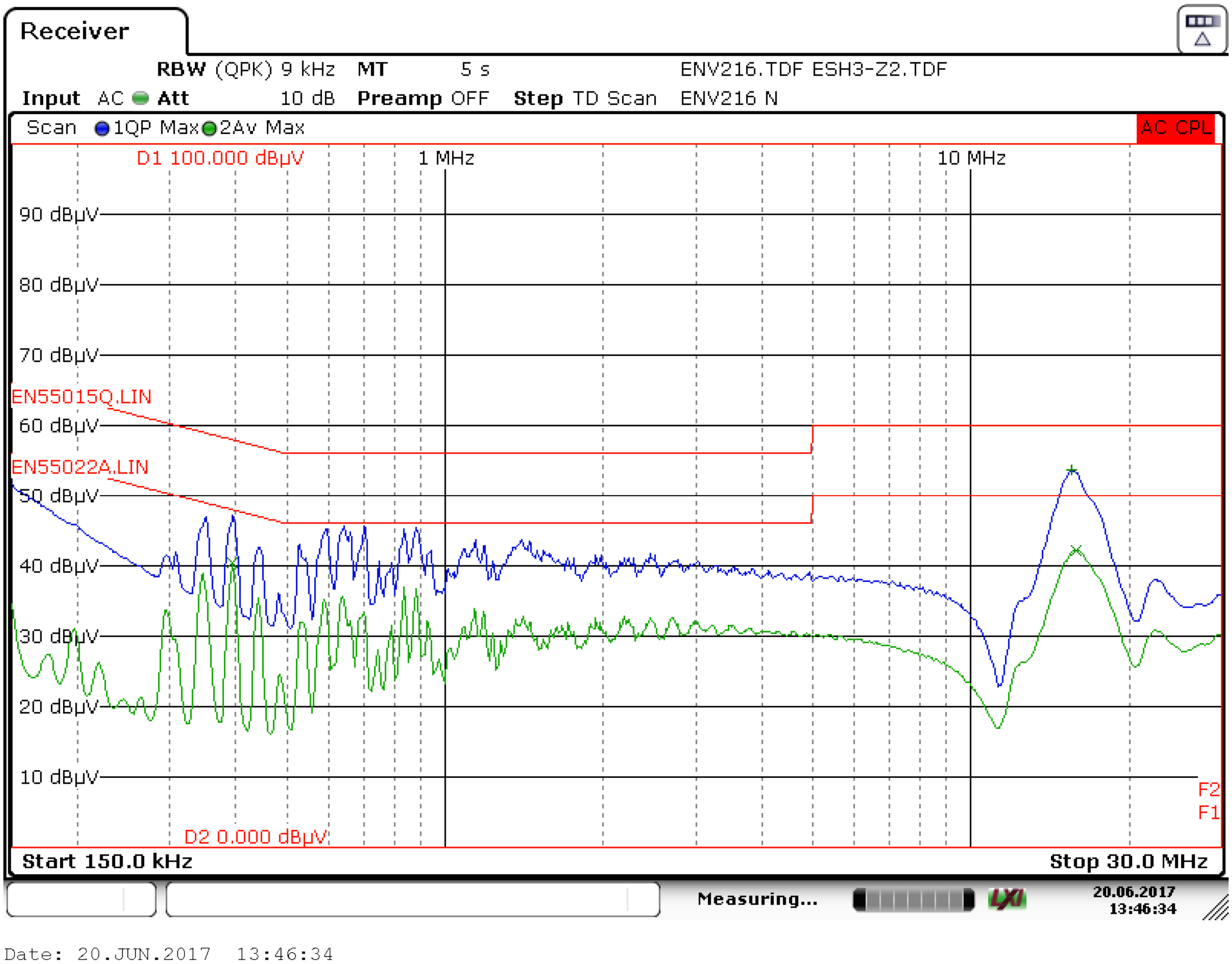


Figure 73 – Floating Negative Output at 230 VAC, Neutral.

12 Line Surge

The unit was subjected to ±3 kV for common mode and ±2 kV for differential mode surge using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

DM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2000	230	L to N	0	Pass
-2000	230	L to N	0	Pass
+2000	230	L to N	90	Pass
-2000	230	L to N	90	Pass
+2000	230	L to N	180	Pass
-2000	230	L to N	180	Pass
+2000	230	L to N	270	Pass
-2000	230	L to N	270	Pass

CM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+3000	230	L/N to PE	0	Pass
-3000	230	L/N to PE	0	Pass
+3000	230	L/N to PE	90	Pass
-3000	230	L/N to PE	90	Pass
+3000	230	L/N to PE	180	Pass
-3000	230	L/N to PE	180	Pass
+3000	230	L/N to PE	270	Pass
-3000	230	L/N to PE	270	Pass

13 Revision History

Date	Author	Revision	Description and Changes	Reviewed
13-Sep-17	CC / DK	1.0	Initial Release.	Apps & Mktg
05-Oct-17	KM	1.1	Updated Schematic, BOM and PCB Image.	
09-Nov-17	KM	1.2	Updated Schematic and Transformer Winding Information.	
20-Jul-18	KM	1.3	Added Magnetics Supplier for T1, L1, and L2	
27-Jul-22	KM	1.4	Updated T1 and the BOM.	

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