Design Example Report

Title	***15 W Tapped Buck Non-Isolated Power Supply Using LinkSwitch™-TN2 LNK3206G***
Specification	90 VAC – 265 VAC Input; 12.0 V / 1 A, 15 V / 200 mA Outputs
Application	Embedded Power Supply
Author	Applications Engineering Department
Document Number	DER-846
Date	March 26, 2020
Revision	1.0

Summary and Features

- Dual output tapped buck topology
- Highly integrated solution
- No optocoupler required for regulation
- >83.5% efficiency at nominal line and full load
- <±5% load regulation
- Low no-load input power <150 mW

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5245 Hellyer Avenue, San Jose, CA 95138 USA.
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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a tapped buck converter designed to provide a non-isolated nominal output voltage of 12 V at 1.0 A load and a secondary output of 15 V at 200mA load from a wide input voltage range of 90 VAC to 265 VAC. This power supply utilizes the LNK3206G from the LinkSwitch-TN2 family of ICs.

This document contains the complete power supply specifications, bill of materials, transformer construction, circuit schematic and printed circuit board layout, along with performance data and electrical waveforms.

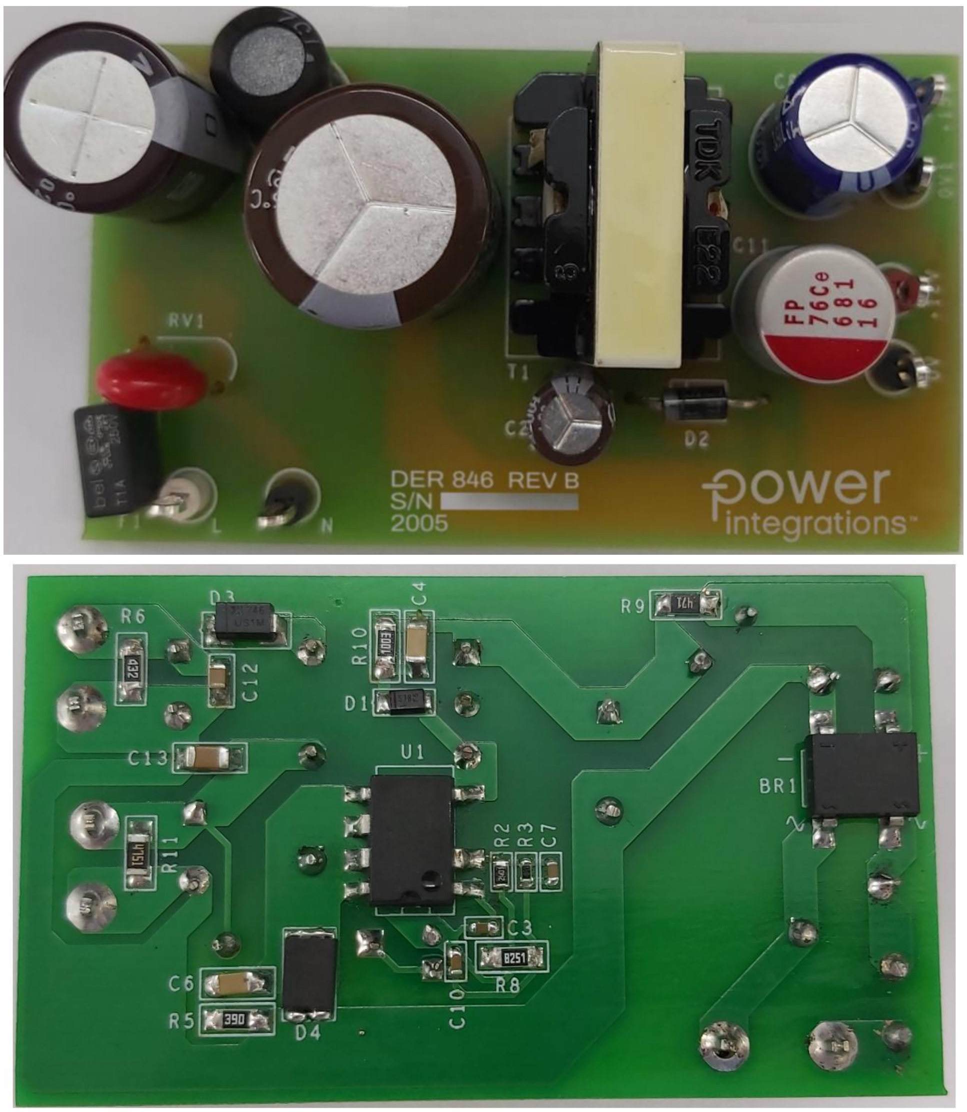

Figure 1 – Populated Circuit Board.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				0.150	W	
Output1						
Output Voltage	V_{OUT}	11.4	12	12.6	V	± 5%
Output Ripple Voltage	V_{RIPPLE}			200	mV	20 MHz Bandwidth.
Output Current	I_{OUT}			1.00	A	
Output2						
Output Voltage	V_{OUT}	14.25	15	15.75	V	± 5%
Output Ripple Voltage	V_{RIPPLE}			200	mV	20 MHz Bandwidth.
Output Current	I_{OUT}			0.2	A	
Total Output Power						
Continuous Output Power	P_{OUT}			15	W	
Efficiency						
Full Load Nominal Input	η	83.5			%	Measured at P_{OUT} 25 °C.
Required average efficiency at 25, 50, 75 and 100 % of P_{OUT}	η_{DOE}	76.41			%	Measured at Nominal Input 115 VAC and 230 VAC.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Surge (Differential)				1	kV	1.2/50 μs Surge, IEC 61000-4-5, Series Impedance: Differential Mode: 2 Ω
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

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3 Schematic

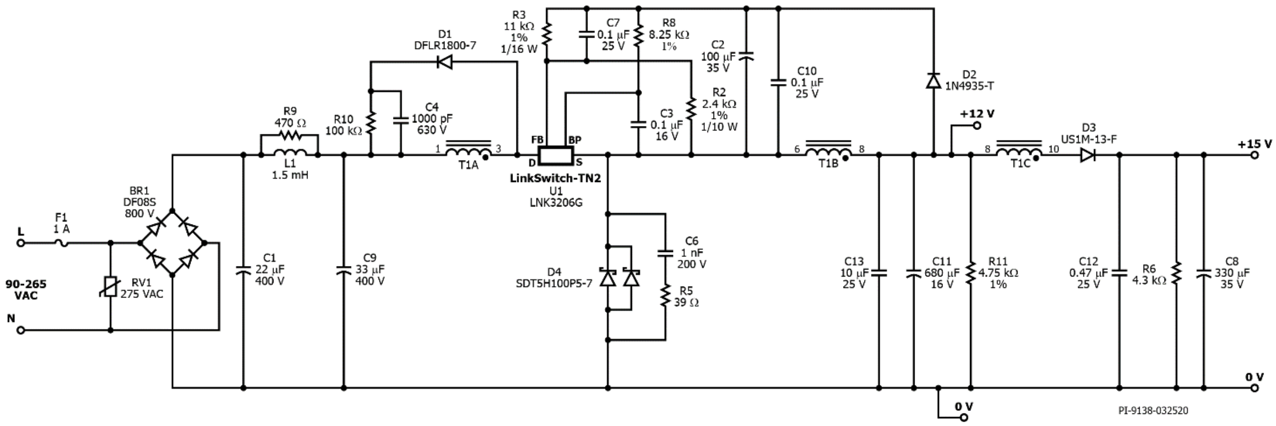

Figure 2 – Schematic.

4 Circuit Description

Buck converter high output current application are limited. Buck integrated power mosfet and controller IC should have greater than 1A current limit in order to support high output current application. High output current will result to increase power loss. Consequently, Increase power loss will yield to high thermals. Proper heatsinking should be implemented for buck converter high current application. Designer might opt to choose a design using PWM controller IC and a large expensive power MOSFET to address thermal concerns. To solve the limitation of integrated IC solution, a tapped-buck converter can be used.

LinkSwitch-TN2 is an excellent choice for a tapped buck configured converter. LNK3206G combines a high voltage power Mosfet, oscillator, simple On/Off control scheme, a high-voltage switched current source for self-biasing, frequency jittering, cycle-by-cycle current limit, and hysteretic thermal shutdown in a single SMD-8C package. The LNK3206G IC was used in a non-isolated tapped buck converter with dual output (main output 12 V and second output 15 V) delivering 1 A and 200 mA respectively.

4.1 *Tapped Buck Configuration*

Conventional tapped buck converter requires additional bias winding and optocoupler circuit since source pin is floating. The tapped buck configuration in this report (T1A to LNK3206G to T1B) eliminates the need of an additional bias winding and optocoupler circuit. Since, the freewheeling diode is connected to the source pin.

4.2 *Input Rectifier and Filter*

Fuse F1 isolates the circuit and provides protection from component failure. Varistor VR1 protects the circuit from excessive input line transient voltages (surge). Bridge rectifier BR1 converts the AC line voltage into the DC voltage seen across capacitors C1 and C9. A pi-filter is formed from differential mode choke L1 and bulk capacitors C1 and C9, providing filtering for differential mode noise.

4.3 *Power Stage*

The LinkSwitch-TN2 IC was utilized and configured as a high-side driver. The LNK3206G IC was selected to deliver typical power of 15 W. When the power MOSFET switches ON, current ramps up and flows through the inductor T1A, T1B and through the main output. Freewheeling diode D4 and D3 are reverse biased. The capacitor C3, connected to the BYPASS pin is charged. The current continues to ramp up until it reaches the current limit set by capacitor C3, which causes the power MOSFET to turn-off. When the power MOSFET switches OFF, the energy in T1 couples through to the main output and second output. The peak current in the output winding steps up by the inductor ratio. This stepped current flows out of the output winding, through freewheeling diode D4, and back through the load. Second output rectification is provided by diode D3.

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The IC is self-starting, using an internal high-voltage current source to charge the BYPASS (BP) pin capacitor, C3, when AC is first applied. At normal operation the primary side block is powered from the main output via circuit, D2 and R8 during switch off-time.

The leakage energy in the T1 causes Drain voltage spikes. The Drain voltage spikes should be limited to less than 90% of the breakdown voltage rating. To minimize the leading edge spikes, a snubber circuit consisting of RCD (D1, C4, and R10) is used. Ringing on the Drain voltage can be minimized by optimizing the snubber design.

The freewheeling diode, D4, should be a Schottky or ultrafast type. Reverse recovery time trr <35 ns should be used. Continuous mode of operation will always occur during start-up thus using slower diodes are not acceptable because it will provide high leading edge current spikes, terminating the operation and preventing the output from reaching its regulation.

4.4 *Output Side and Feedback Loop*

The sudden current step in the inductor during off time will create a high ripple current in the output capacitor. This will translate to high output voltage ripple. Main output capacitor C11 and second output capacitor C8 are selected to have a very low ESR capacitor to minimize the output ripple. Additional ceramic capacitor C13 and C12 further helps to reduce output ripple.

The feedback loop is formed by D2, R2 and R3 Resistors R2 and R3 are configured to deliver an output voltage of 12 V.

4.5 *Secondary Output Winding*

To create a secondary output, T1C winding, D3, and C8 were added to the main output. Second output winding T1C was designed to produce an additional voltage on top of the main output. Voltage develop across T1C plus the main output provides the second output voltage. The second output winding T1C was computed based on the transformer voltage turns ratio (main output, second output, and T1B). Diode drop across the freewheeling diodes D4 and D3 were also considered in the design of the T1C winding turns.

5 PCB Layout

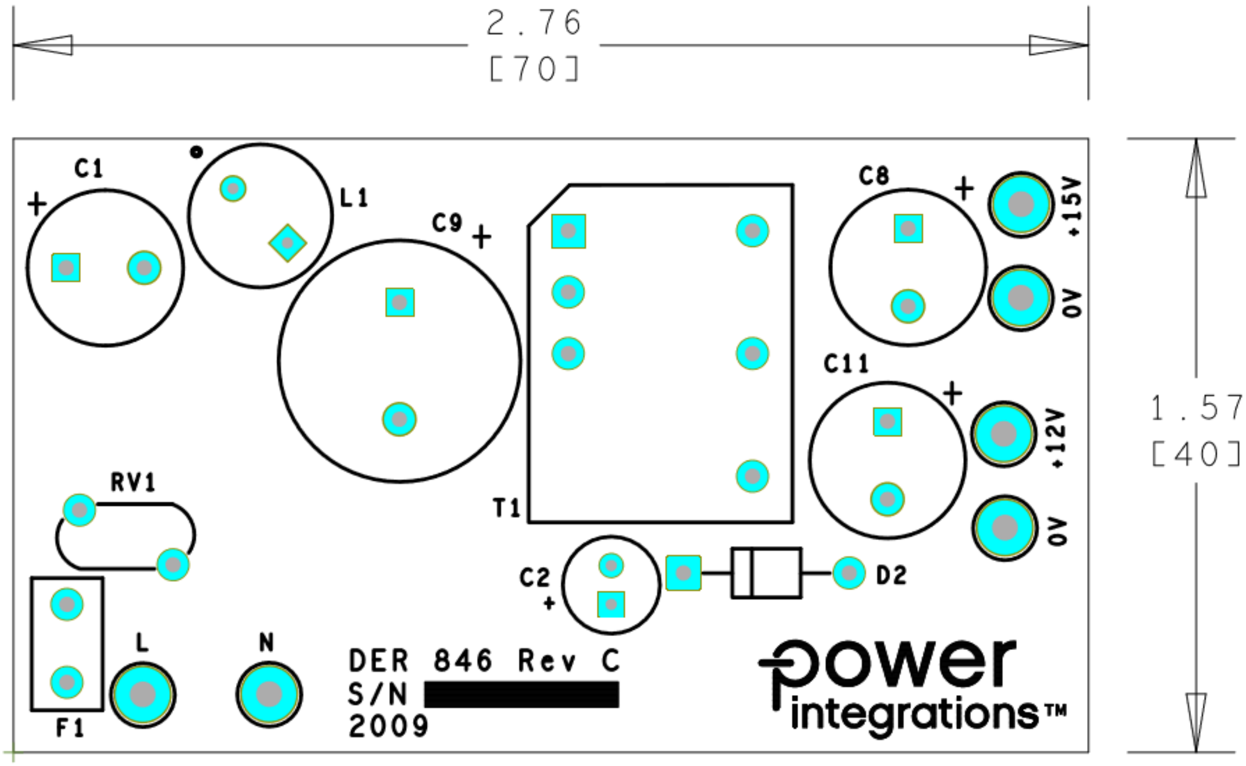

Figure 3 – Printed Circuit Board, Top View.

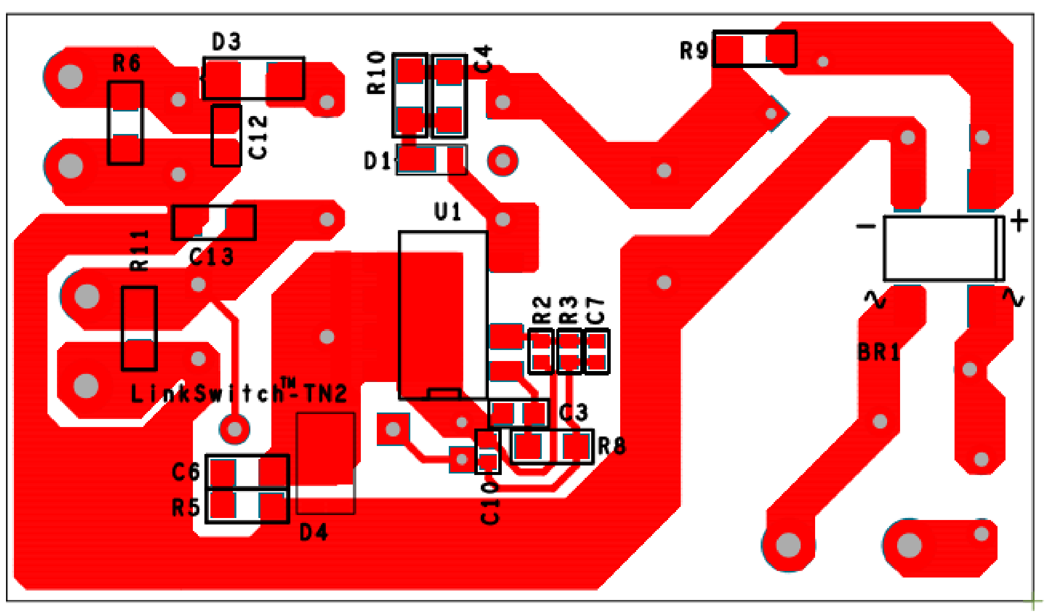

Figure 4 – Printed Circuit Board, Bottom View.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	800 V, 1 A, Bridge Rectifier, SMD, DFS	DF08S	Diodes, Inc.
2	1	C1	22 μF, 400 V, Electrolytic, (12.5 x 20)	UCS2G220MHD	Nichicon
3	1	C2	100 μF, 35 V, Electrolytic, Gen. Purpose, (6.3 x 11)	EKMG350ELL101MF11D	Nippon Chemi-Con
4	1	C3	0.1 μF, ±5%, 16V, X7R, 0805	C0805C104J4RACTU	Kemet
5	1	C4	1000 pF, 630 V, Ceramic, X7R, 1206	C1206C102KBRACTU	Kemet
6	1	C6	1 nF, 200V, 10%, Ceramic, X7R, 1206	12062C102KAT2A	AVX
7	1	C7	0.1 μF, 25 V, Ceramic, X7R, 0603	VJ0603Y104KXXAC	Vishay
8	1	C8	330 μF, 35 V, Electrolytic, Low ESR, 68 mΩ, (10 x 16)	ELXZ350ELL331MJ16S	Nippon Chemi-Con
9	1	C9	33 μF, 400 V, Electrolytic, Low ESR, 901 mΩ, (16 x 20)	EKMX401ELL330ML20S	Nippon Chemi-Con
10	1	C10	0.1 μF, 25 V, Ceramic, X7R, 0603	VJ0603Y104KXXAC	Vishay
11	1	C11	680 μF, 20%,16 V, Aluminum Polymer Electrolytic, Very Low ESR, 10 mΩ, 2000 Hrs @ 105°C, (10 x 14)	RNU1C681MDN1PH	Nichicon
12	1	C12	0.47 μF, ±10%,25 V, Ceramic, X7R, 0805	CGA4J2X7R1E474K125AA	TDK
13	1	C13	10 μF, 25 V, Ceramic, X7R, 1206	C3216X7R1E106M160AB	TDK
14	1	D1	800 V, 1 A, Rectifier, POWERDI123	DFLR1800-7	Diodes, Inc.
15	1	D2	200 V, 1 A, Fast Recovery, 200 ns, DO-41	1N4935-T	Diodes, Inc.
16	1	D3	1000 V, 1 A, Ultrafast Recovery, GPP, DO-214AC SMA	US1M-13-F	Diodes, Inc.
17	1	D4	100 V, 5 A, Schottky, SMD, POWERD15,PowerDI™ 5	SDT5H100P5-7	Diodes, Inc.
18	1	F1	1 A, 250 V, Slow, Long Time Lag, RST 1	RST 1	Belfuse
19	1	L1	INDUCTOR, FIXED, 1.5MH, 430 mA, 3.8 OHM, TH	RLB9012-152KL	Bourns
20	1	R2	RES, SMD, 2.4 KΩ, 1%, 1/10W, ±100ppm/°C, 0603	RC0603FR-072K4L	Yageo
21	1	R3	RES, 11 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1102V	Panasonic
22	1	R5	RES, 39 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ390V	Panasonic
23	1	R6	RES, 4.3 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ432V	Panasonic
24	1	R8	RES, 8.25 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF8251V	Panasonic
25	1	R9	RES, 470 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ471V	Panasonic
26	1	R10	RES, 100 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ104V	Panasonic
27	1	R11	RES, 4.75 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF4751V	Panasonic
28	1	RV1	275 VAC, 23 J, 7 mm, RADIAL	V275LA4P	Littlefuse
29	1	T1	Bobbin, EE22. Vertical,10 pins	BE-22-1110CPFR	TDK
30	1	U1	LinkSwitch-TN2, SMD-8C	LNK3206G	Power Integrations

Miscellaneous

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	+12V	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
2	1	+15V	Test Point, BLU, THRU-HOLE MOUNT	5127	Keystone
3	1	0V	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
4	1	0V	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
5	1	L	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
6	1	N	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone

7 Transformer Specification

7.1 *Electrical Diagram*

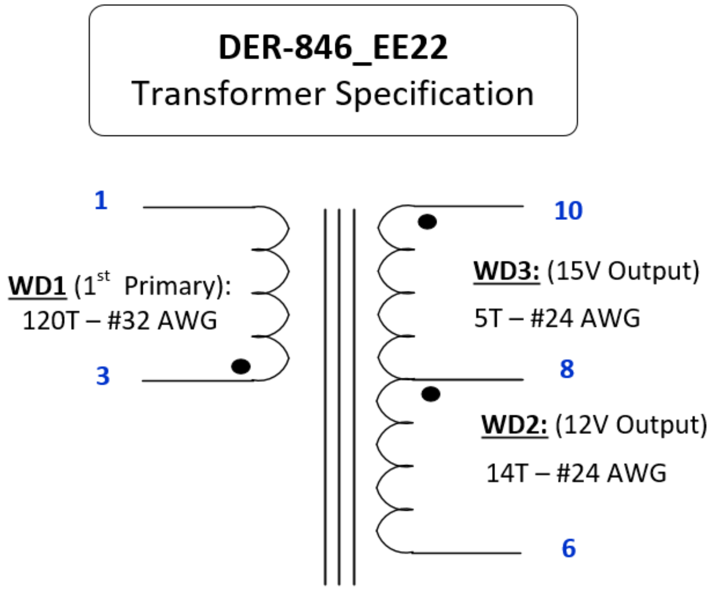

Figure 5 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and pin 3 with all other windings open.	2207 μH
Tolerance	Tolerance of Primary Inductance.	±7%
Leakage Inductance	Measured across primary winding with all other windings shorted.	<70 μH

7.3 *Material List*

Item	Description
[1]	Core: EE22 TDK PC40
[2]	Bobbin: EE2, Vertical, 10 pins,
[3]	Magnet Wire: #24 AWG.
[4]	Magnet Wire: #32 AWG.
[5]	Polyester Tape: 8.5 mm.
[6]	Polyester Tape: 6 mm.
[7]	Varnish: Dolph BC 359 or Equivalent.

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7.4 *Transformer Build Diagram*

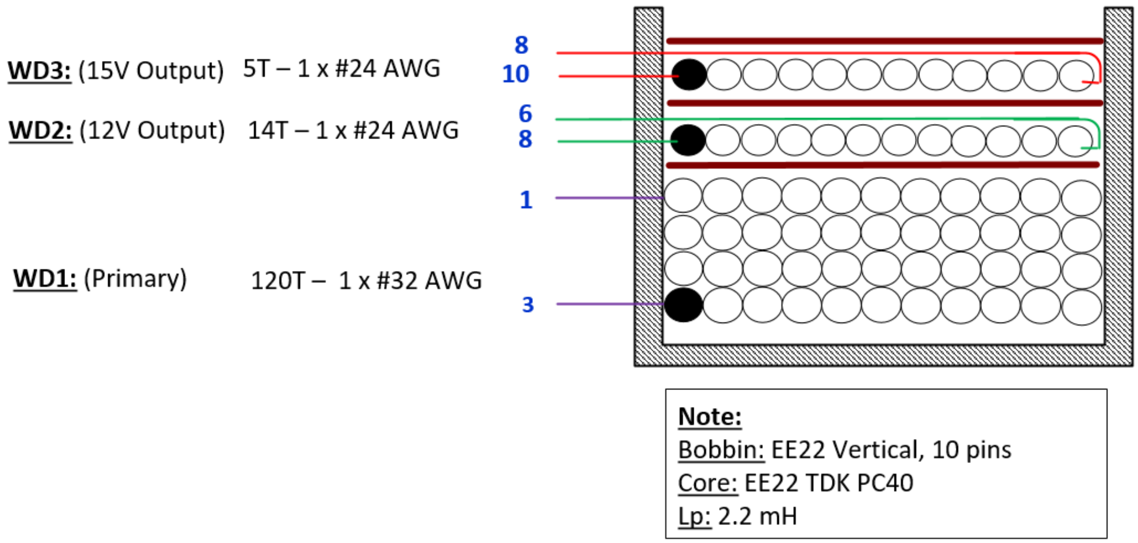
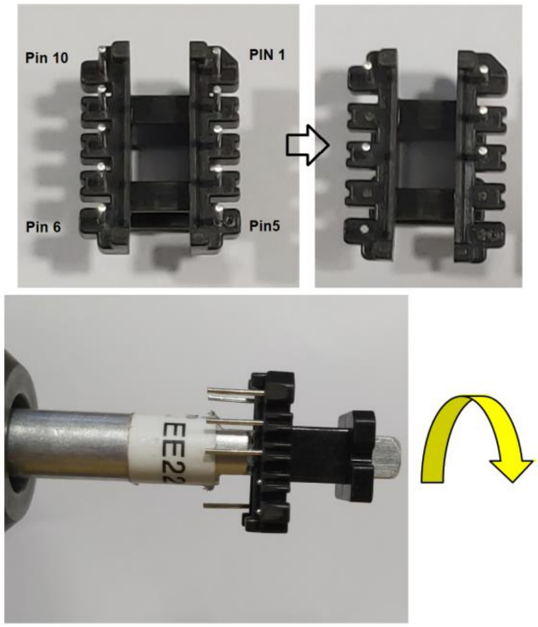
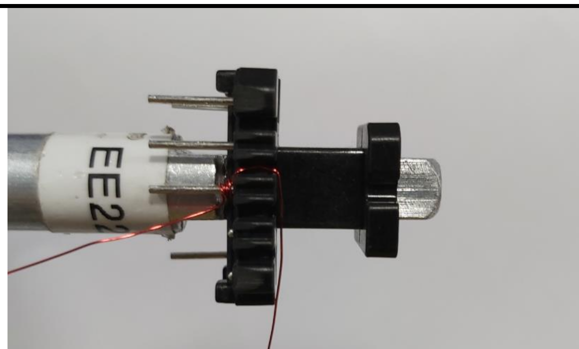
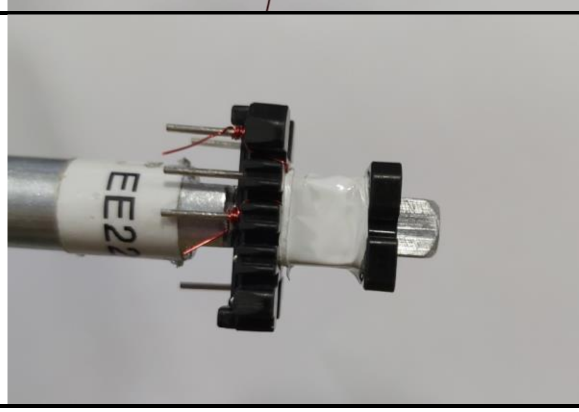


Figure 6 – Transformer Build Diagram.

7.5 *Transformer Instructions*

Bobbin Preparation	For the purposes of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise. Before winding, remove pins 4, 5, 7, and 9.
WD1 Primary	Start at pin 3, wind 120 turns of wire Item [4] in 4 layers. Finish at pin 1
Insulation	Use 1 layer of tape Item [5] for insulation.
WD2 12V Output	Start at pin 8, wind 14 turns of wire Item [3] in 1 layer. Finish at pin 6
Insulation	Use 1 layer of tape Item [5] for insulation.
WD3 15V Output	Start at pin 10, wind 5 turns of wire Item [3] in 1 layer. Finish at pin 8
Insulation	Use 1 layer of tape Item [5] for insulation.
Finish	Gap cores to get 2207 μH. Wrap the body of transformer with 2 layers of tape Item [6]. Varnish using Item [7].

7.6 ***Transformer Winding Illustrations***

Bobbin Preparation		For the purposes of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise. Before winding, remove pins 4, 5, 7, and 9.
WD1 Primary		Start at pin 3, wind 120 turns of wire Item [4] in 4 layers. Finish at pin 1
Insulation		Use 1 layer of tape Item [5] for insulation.

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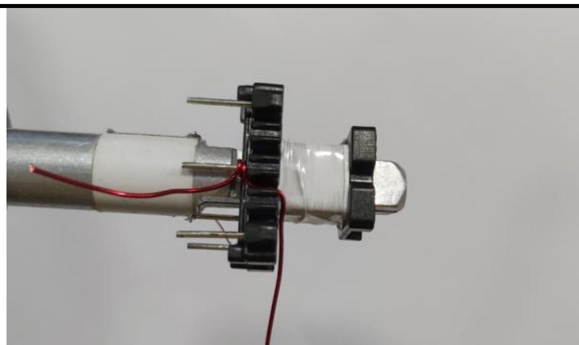
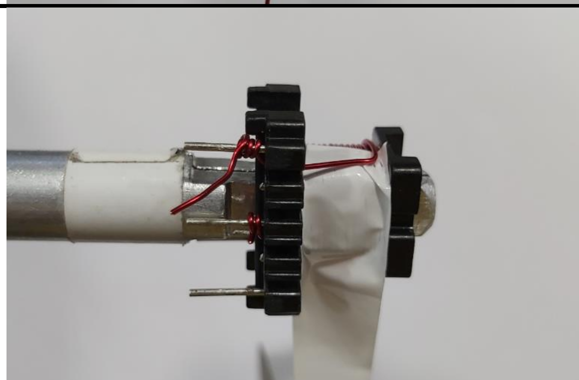
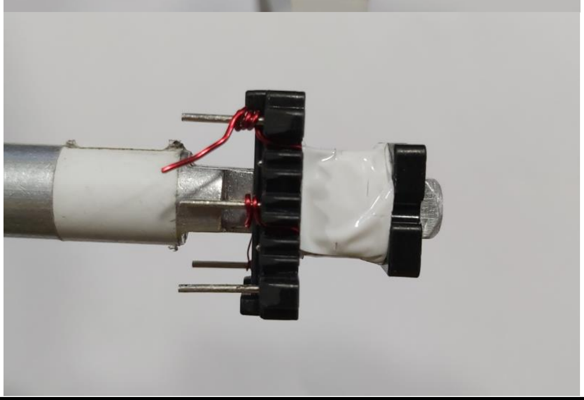
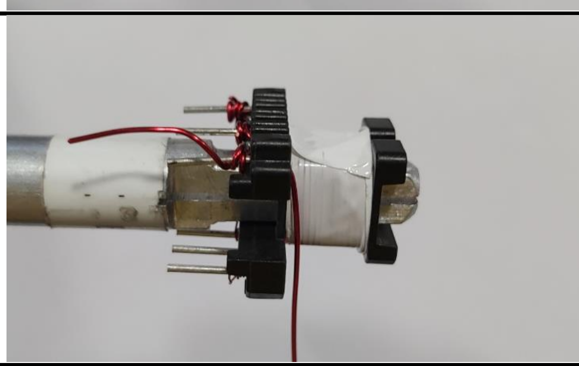
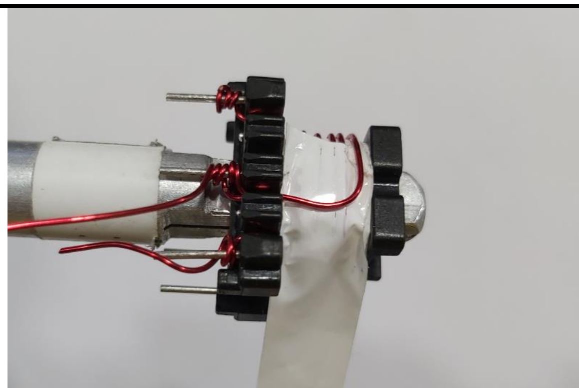
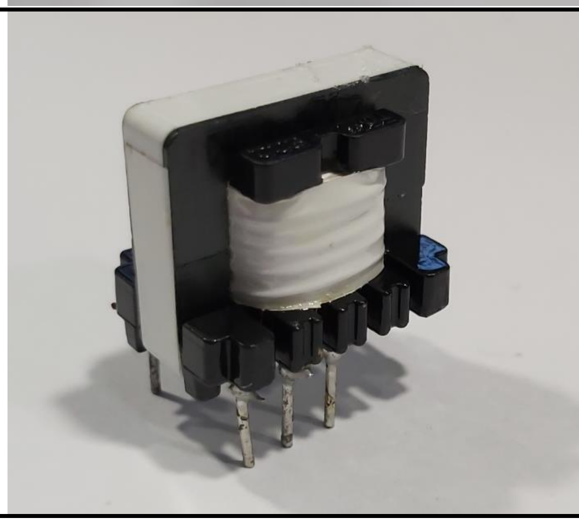
WD2 **12V Output**		Start at pin 8, wind 14 turns of wire Item [3] in 1 layer. Finish at pin 6
Insulation	 	Use 1 layer of tape Item [5] for insulation.
WD3 **15V Output**		Start at pin 10, wind 5 turns of wire Item [3] in 1 layer. Finish at pin 8

Insulation	 	Use 1 layer of tape Item [5] for insulation.
Finish		Gap cores to get 2207 uH. Wrap the body of transformer with 2 layers of tape Item [6]. Varnish using Item [7].

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9 Transformer Design Spreadsheet

ACDC_LinkSwitchTN2_TappedBuck_013120; Rev.0.3; Copyright Power Integrations 2020	INPUT	INFO	OUTPUT	UNIT	LinkSwitchTN2 Tapped Buck Spreadsheet
APPLICATION VARIABLES					
VACMIN	90		90	V	Minimum AC input voltage
VACMAX			265	V	Maximum AC input voltage
VAC_RANGE			UNIVERSAL		AC line voltage range
FL			50	Hz	AC line voltage frequency
LINE_RECTIFICATION	F		F		Select F (full) or H (half) wave rectification
VOUT			12.00	V	Output voltage
IOUT	1.25	Warning	1.25	A	Output current cannot be delivered across all line and tolerance corners. Lowest current delivered is 1.067A. Decrease KP
POUT			15.00	W	Output power
N	0.84		0.84		DCDC efficiency estimate (after bulk cap to output terminals)
CIN	55.00		55.00	uF	Input capacitance is set to 2 uF/W
VF_BRIDGE			0.70	V	Bridge rectifier forward voltage drop (per diode)
DC INPUT VOLTAGE PARAMETERS					
VMIN			104.77	V	Minimum DC input voltage
VMAX			373.37	V	Maximum DC input voltage
ENTER LINKSWITCH-TN2 VARIABLES					
CURRENT LIMIT MODE	STD		STD		Choose 'RED' for reduced current limit or 'STD' for standard current limit
PACKAGE	SMD-8C		SMD-8C		Select the device package
DEVICE SERIES	LNK3206		LNK3206		Generic LinkSwitch-TN2 device
DEVICE CODE			LNK3206G		Required LinkSwitch-TN2 device
ILIMITMIN			0.450	A	Minimum current limit of the device
ILIMITTYP			0.482	A	Typical current limit of the device
ILIMITMAX			0.515	A	Maximum current limit of the device
FSMIN			62000	Hz	Minimum switching frequency
FSTYP			66000	Hz	Typical switching frequency
FSMAX			72000	Hz	Maximum switching frequency
KP	0.590		0.590		Ripple to peak current ratio at VMIN
DMAX			0.569		Duty ratio at full load, minimum primary inductance and minimum input voltage
T_ON_MIN			2.571	us	Worst-case minimum on-time
VDSON_SWITCH			2.00	V	MOSFET on-time drain to source voltage estimate
RDSON_SWITCH			12.90	ohms	MOSFET on-time drain to source resistance at 100degC
VDSOFF_SWITCH			625.31	V	MOSFET off-time drain to source voltage estimate
IPEAK_SWITCH			0.515	A	MOSFET peak current
IAVE_SWITCH			0.207	A	MOSFET average current
IRMS_SWITCH			0.282	A	MOSFET RMS current
INDUCTOR CONSTRUCTION VARIABLES					

CORE_SHAPE	EE22		EE22		Core shape
CORE_CODE			PC40EE22-Z		Core code
AE			41.00	mm^2	Core effective cross-sectional area
LE			39.60	mm^2	Core effective path length
VE			1620	mm^2	Core effective volume
AL			2180	nH/turn^2	Ungapped core effective AL value
BOBBIN			BE22-118 CPFR		Core bobbin
BW			8.45	mm	Bobbin physical winding width
AW			20.00	mm^2	Bobbin window area
BW_MARGIN			0.00	mm	Total margin from sides of bobbin to actual winding
INDUCTOR DESIGN PARAMETERS					
L_TOL	7.00		7.00	%	Inductance tolerance
L_MIN			2053.22	uH	Minimum inductance (sum of input and output winding inductances)
L_TYP			2207.76	uH	Typical inductance (sum of input and output winding inductances)
L_MAX			2362.31	uH	Maximum inductance (sum of input and output winding inductances)
N_RATIO	8.600		8.600		Target turns ratio: input turns : output turns
N_TOTAL	134		134	turns	Total number of turns
N1			120	turns	Number of turns in input winding.
N2			14	turns	Number of turns in output winding.
N_RATIO_ACTUAL			8.571		Calculated turns ratio: input turns : output turns
BM		Warning	2214.4	Gauss	The maximum flux density is higher than 2000 Gauss. This may lead to audible noise or core saturation
BAC			1107.2	Gauss	Maximum operating AC flux density
ur			94.50		Relative permeability of gapped core
LG			0.395	mm	Core gap length
FIT FACTOR			82.27	%	Percentage fill of winding window
Input Section					
N1			120	turns	Number of turns in input winding.
IRMS_N1			0.282	A	RMS current flowing through input winding
AWG_N1	Auto		32	AWG	Target wire gauge for the input winding
LAYERS_N1			3.47	layers	Number of laters for input winding
CMA_N1			224	Cmils/A	Input winding current capacity (200 < CMA < 500)
Output Section					
N2			14	turns	Number of turns in output winding.
IRMS_N2			1.724	A	RMS current flowing through output winding
AWG_N2	Auto		24	AWG	Target wire gauge for the output winding
LAYERS_N2			1.35	layers	Number of laters for output winding
CMA_N2			234	Cmils/A	Output winding current capacity (200 < CMA < 500)
TAPPED INDUCTOR BUCK DIODE					

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VF_DIODE			0.500	V	Tapped winding diode forward voltage drop
IPEAK_DIODE			4.929	A	Tapped winding diode peak current
IAVE_DIODE			1.804	A	Tapped winding diode average current
IRMS_DIODE			2.435	A	Tapped winding diode RMS current
PIV_DIODE			49.546	V	Tapped winding diode peak inverse voltage without parasitic ring
DIODE			ES2B		Recommended tapped winding diode
VRRM_DIODE			100	V	VRRM of recommended tapped winding diode
IF_DIODE			2.000	A	Average forward current of recommended tapped winding diode
TRR_DIODE			35	ns	Reverse recovery time of recommended tapped winding diode
OUTPUT CAPACITOR					
IRIPPLE_COUT			2.097	A	Output capacitor ripple current
FEEDBACK PARAMETERS					
RLOWER			2490	Ohm	Upper resistor in feedback resistor divider network
RUPPER			11500	Ohm	Lower resistor in feedback resistor divider network

Note:

Io Warning – Inductor power delivery was computed based on all input lines and tolerances. Using the lowest input line and lowest tolerances resulted to a warning. There is a low probability of low input and low tolerances will occur at the same time.

Bm Warning – This warning was trigger due to audible noise mitigation. Since audible noise is not a requirement for this application, flux density of 2214.4 G is accepted. Since flux density is below 3000 G, core saturation is not a problem.

The two output tapped buck calculations were performed by assuming a single output tapped buck topology and aggregating the total power of the two windings into a single winding for simplicity.

The number of turns of the secondary winding was calculated based on the voltage difference between the two output voltages and using the transformer voltage turns ratio equation.

$$\frac{N_{T1B}}{(Vo_{main}+V_{D4})} = \frac{N_{T1C}}{((Vo_2+V_{D3})-Vo_{main})}$$

10 Performance Data

10.1 *Efficiency*

10.1.1 Average Efficiency at 115 VAC

Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT1} at PCB (V_{DC})	I_{OUT1} (A_{DC})	P_{OUT1} (W)	V_{OUT2} at PCB (V_{DC})	I_{OUT2} (A_{DC})	P_{OUT2} (W)	Efficiency at PCB (%)
100%	115	326.60	17.38	11.71	999.80	11.71	15.02	199.57	3.00	84.61
75%	115	260.30	13.05	11.73	749.90	8.79	15.04	149.65	2.25	84.62
50%	115	195.97	8.74	11.75	499.90	5.88	15.07	99.67	1.50	84.39
25%	115	136.40	4.44	11.80	249.95	2.95	15.15	49.69	0.75	83.33
									Average	**84.24**

10.1.2 Average Efficiency at 230 VAC

Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT1} at PCB (V_{DC})	I_{OUT1} (A_{DC})	P_{OUT1} (W)	V_{OUT2} at PCB (V_{DC})	I_{OUT2} (A_{DC})	P_{OUT2} (W)	Efficiency at PCB (%)
100%	230	190.26	17.15	11.73	999.90	11.73	15.05	199.60	3.00	85.89
75%	230	150.74	12.89	11.74	750.00	8.81	15.06	149.62	2.25	85.80
50%	230	110.77	8.65	11.77	500.00	5.88	15.08	99.66	1.50	85.37
25%	230	68.16	4.44	11.82	249.97	2.95	15.14	49.74	0.75	83.34
									Average	**85.10**

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10.1.3 Full Load Efficiency vs. Line

Test Condition: Soak for 15 minutes for each line.

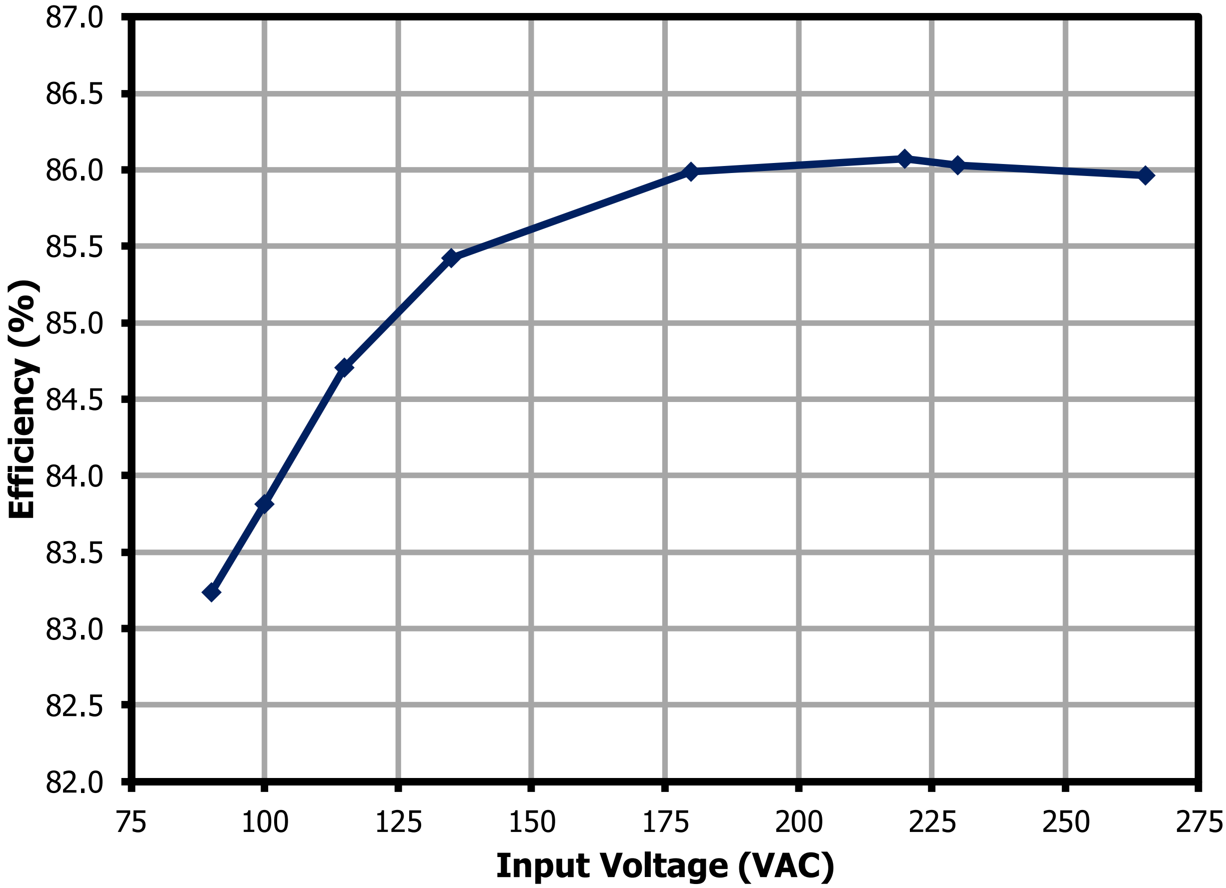

Figure 7 – Efficiency vs. Input Voltage

10.1.4 Efficiency vs. Load

Test Condition: Soak for 15 minutes each line, and 5 minutes for each load.

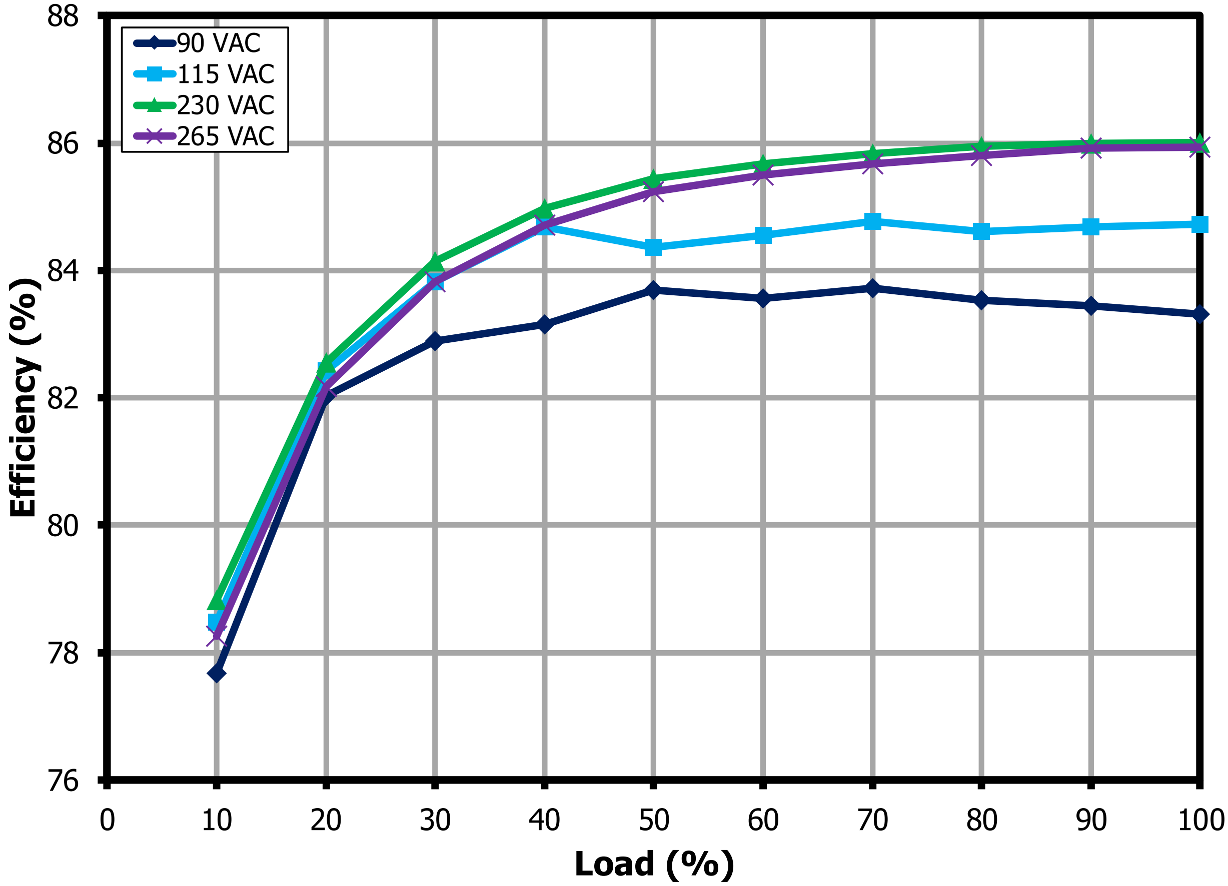

Figure 8 – Efficiency vs. Percentage Load.

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10.2 ***No-Load Input Power***

Test Condition: Soak for 15 minutes each line and 1 minute integration time.

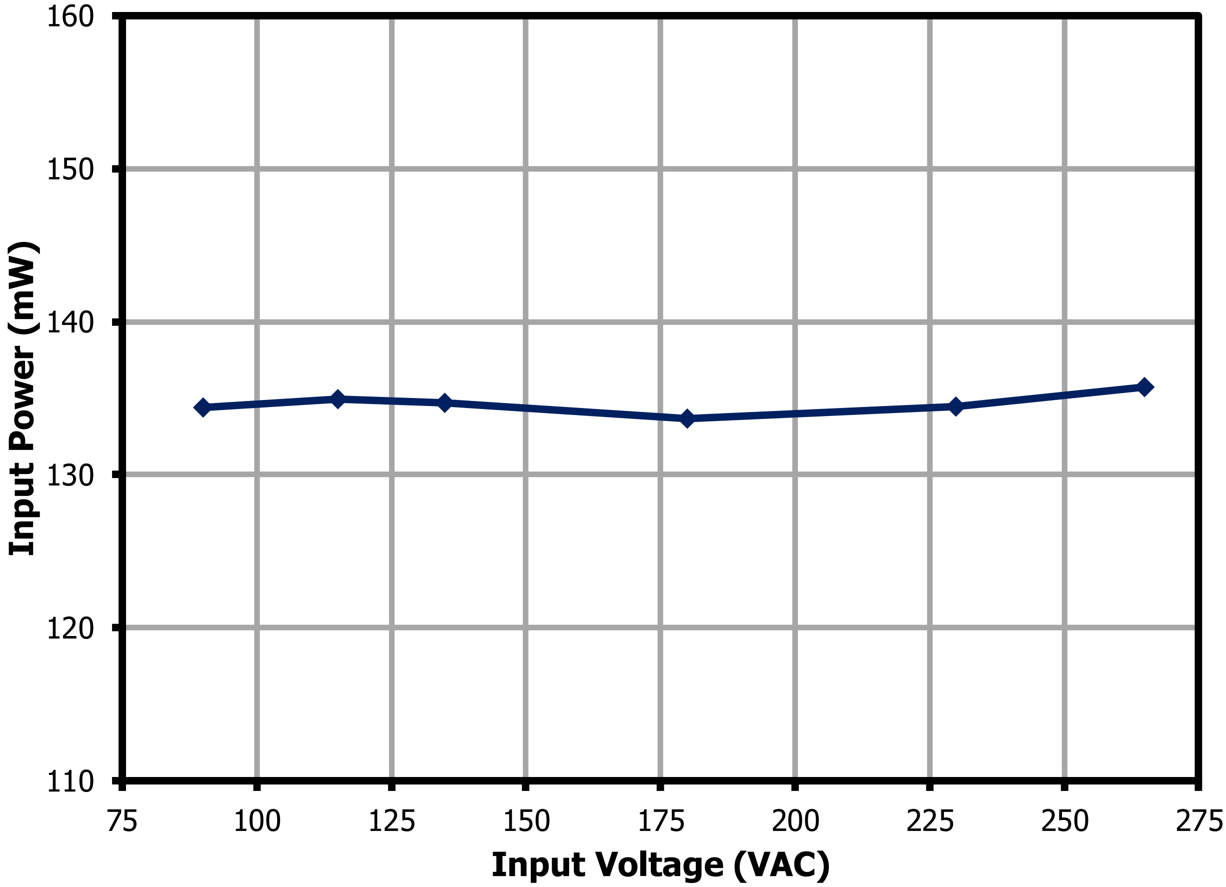

Figure 9 – No-Load Input Power vs. Line at Room Temperature.

10.3 *Line Regulation*

Test Condition: Soak for 15 minutes for each line.

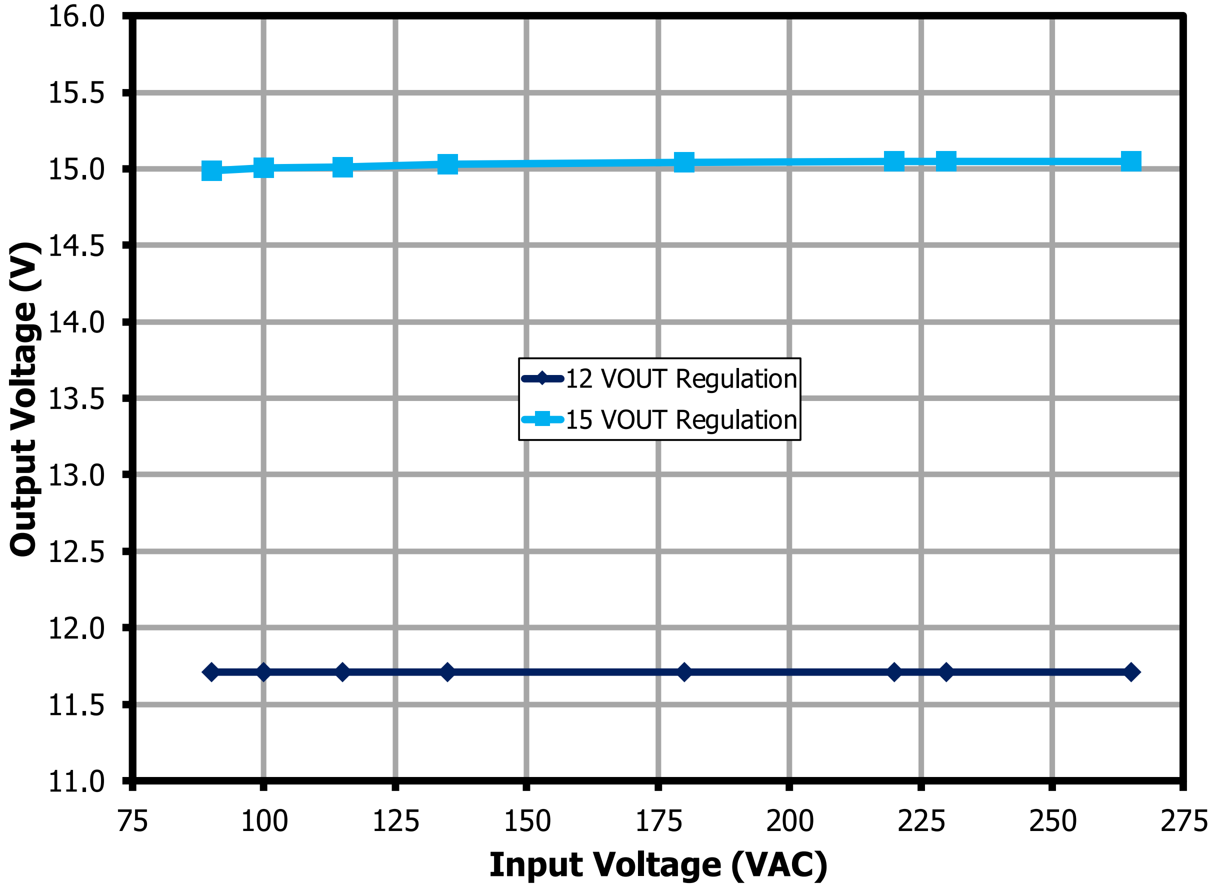

Figure 10 – Output Voltage vs. Line Voltage.

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10.4 *Load Regulation*

Test Condition: Soak for 15 minutes each line, and 5 minutes for each load.

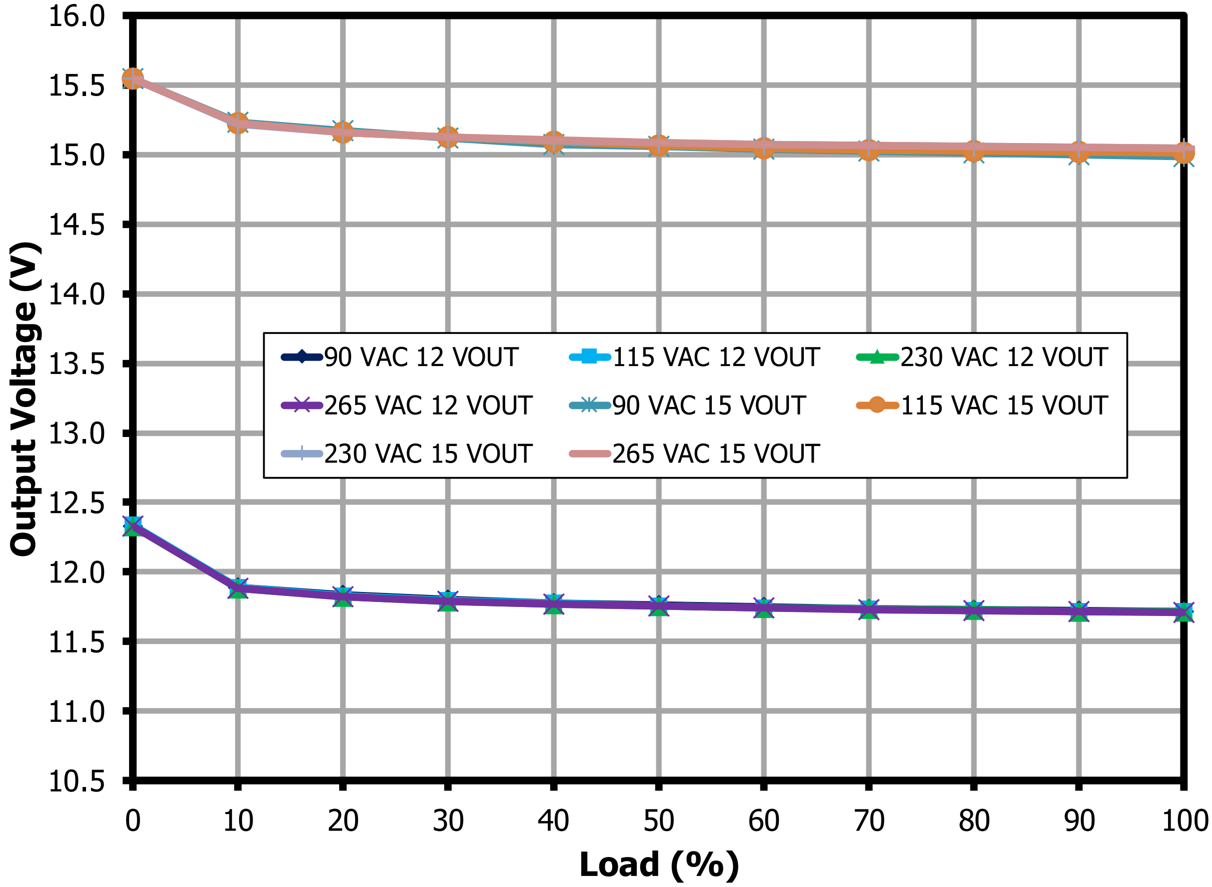

Figure 11 – Output Voltage vs. Percent Load.

10.5 ***Output Cross Regulation***

10.5.1 Cross Regulation 15 V at 90 VAC

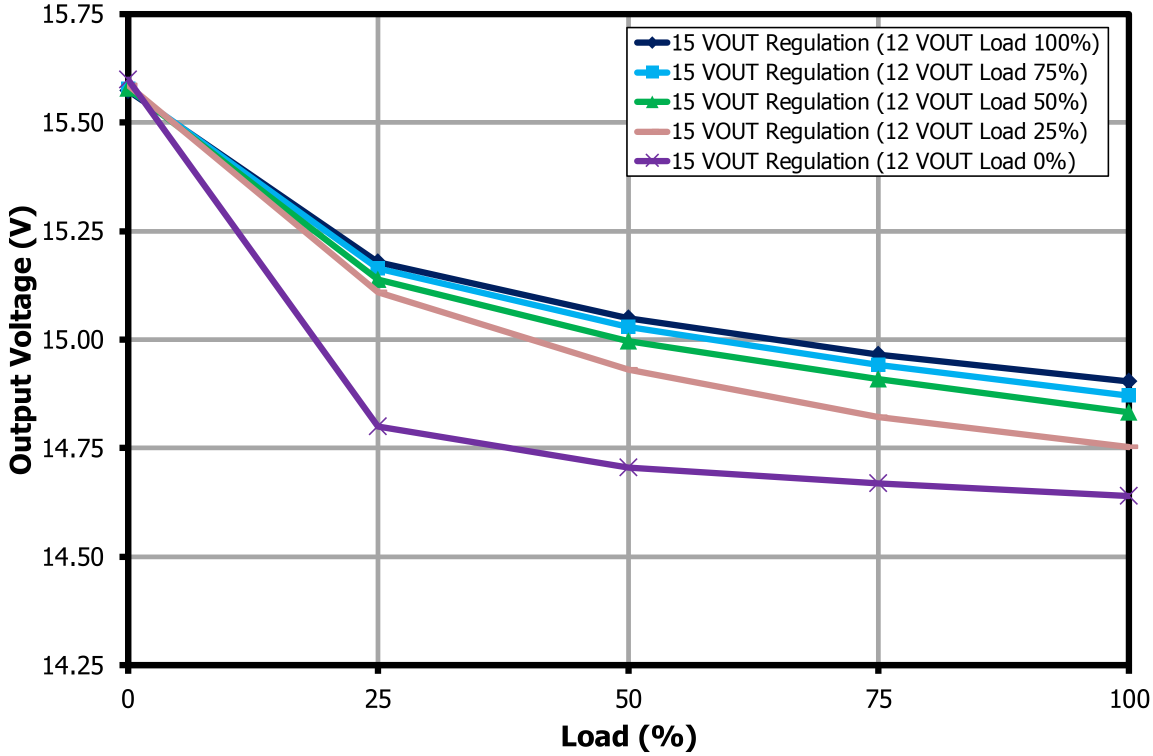

Figure 12 – Output Voltage vs. Percent Load.

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10.5.2 Cross Regulation 15 V at 115 VAC

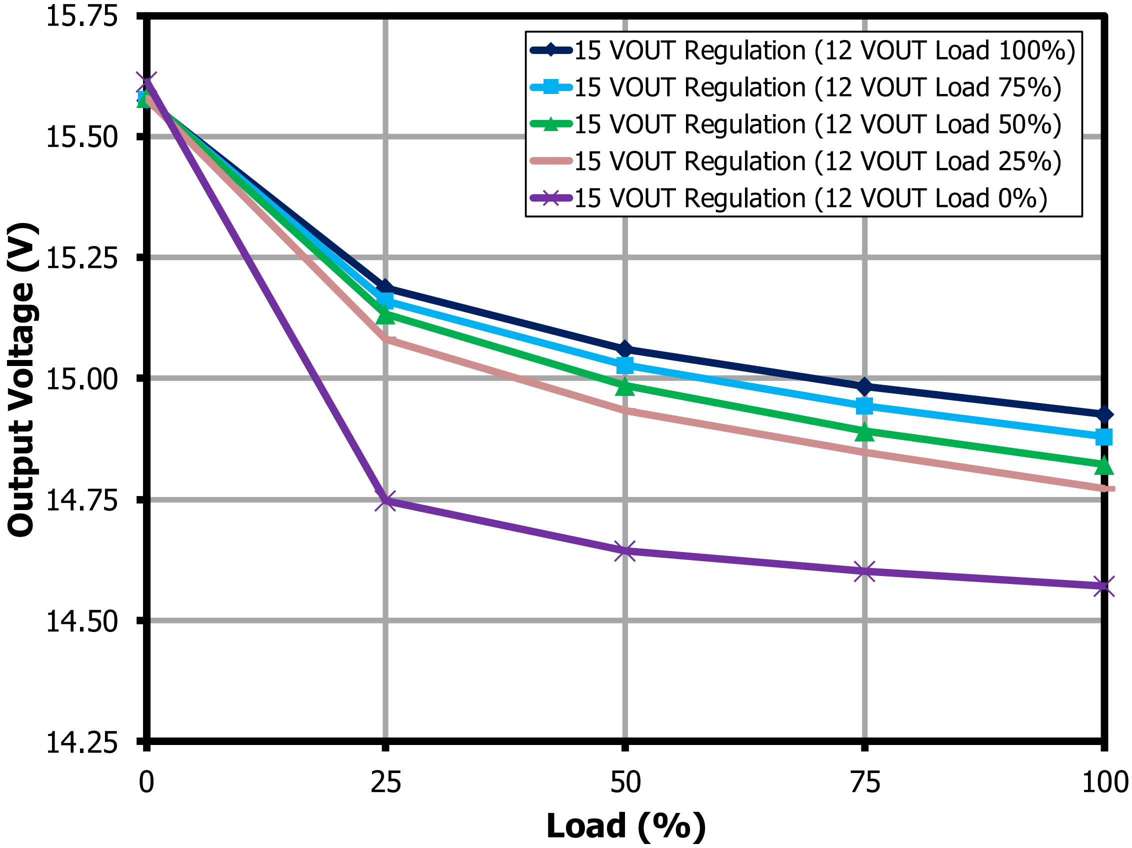

Figure 13 – Output Voltage vs. Percent Load.

10.5.3 Cross Regulation 15 V at 230 VAC

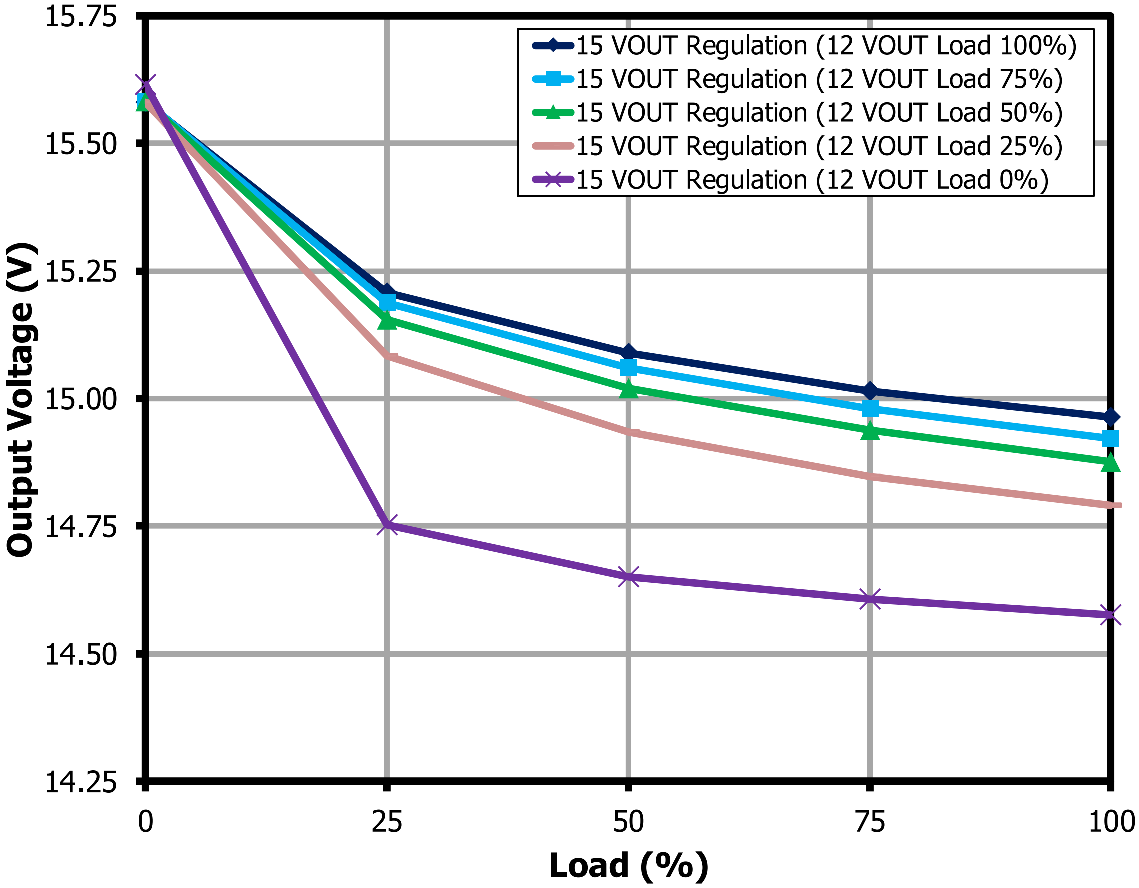

Figure 14 – Output Voltage vs. Percent Load.

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10.5.4 Cross Regulation 15 V at 265 VAC

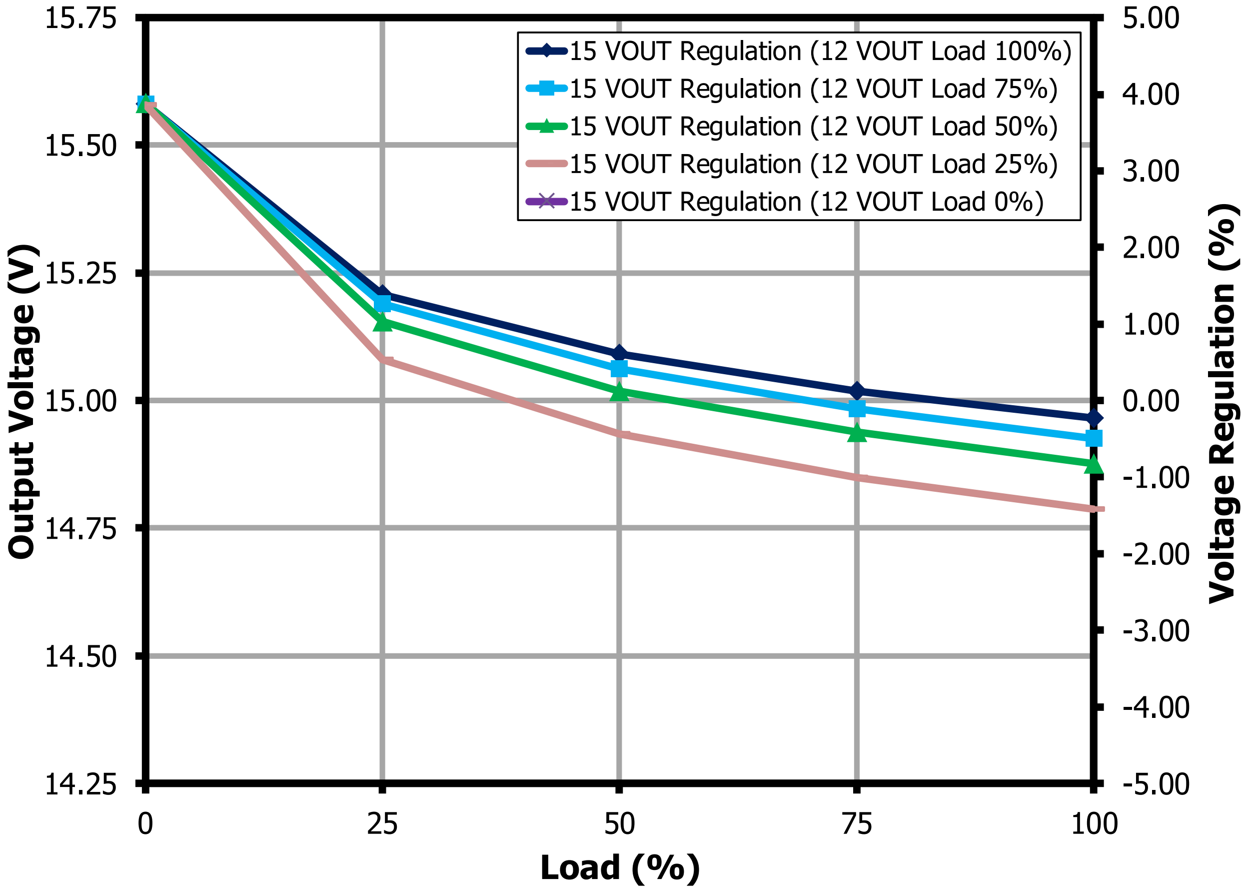

Figure 15 – Output Voltage vs. Percent Load.

10.5.5 Cross Regulation 12 V at 90 VAC

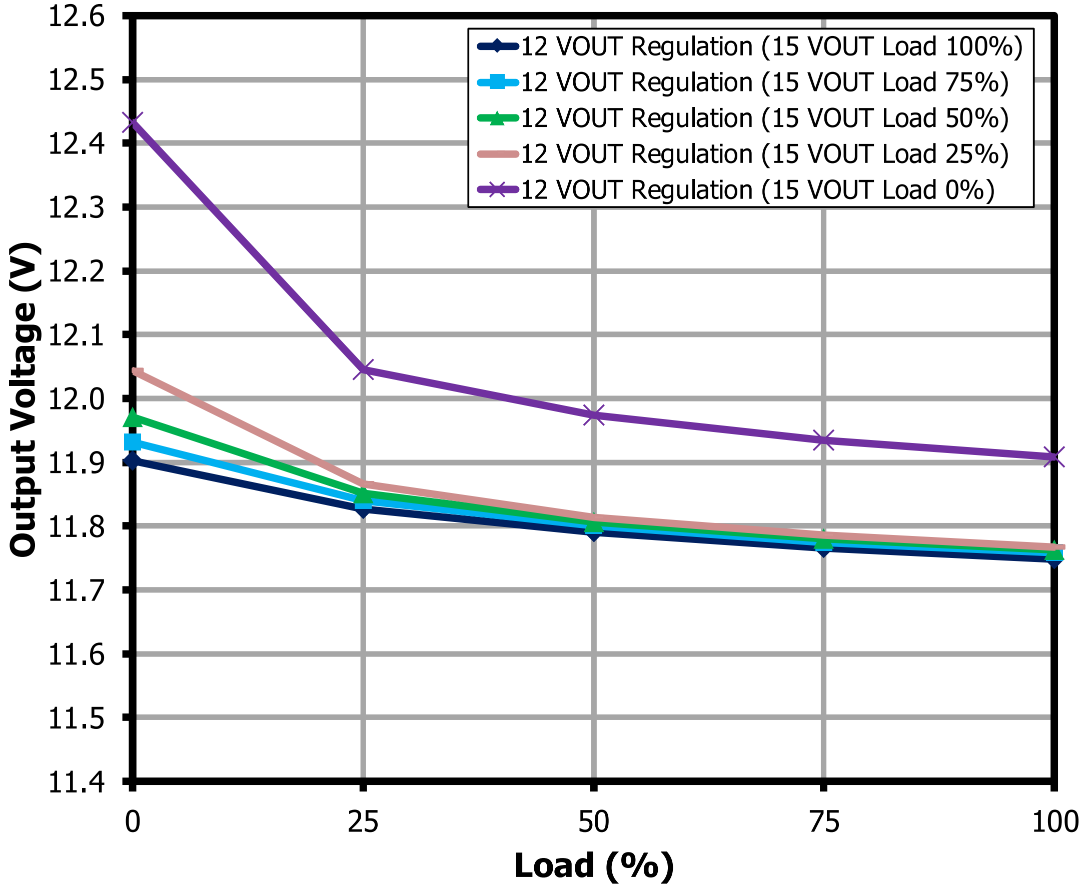

Figure 16 – Output Voltage vs. Percent Load.

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10.5.6 Cross Regulation 12 V at 115 VAC

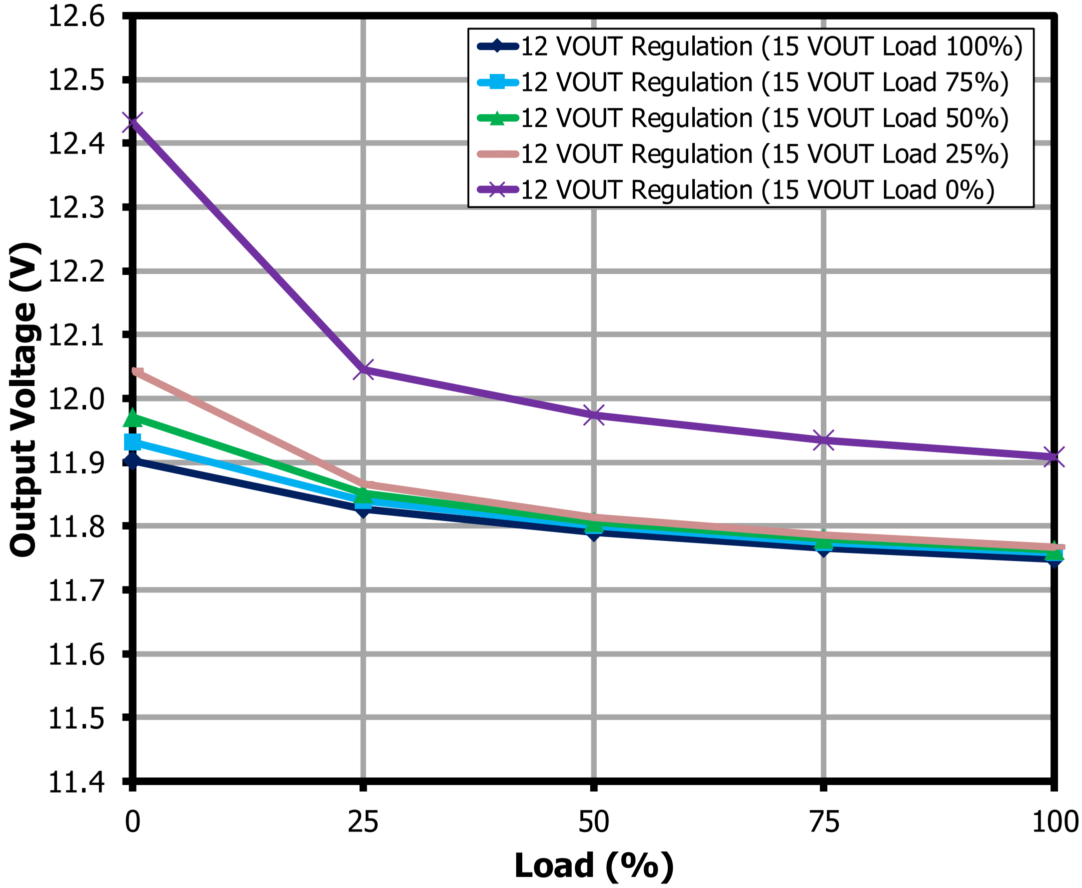

Figure 17 – Output Voltage vs. Percent Load.

10.5.7 Cross Regulation 12 V at 230 VAC

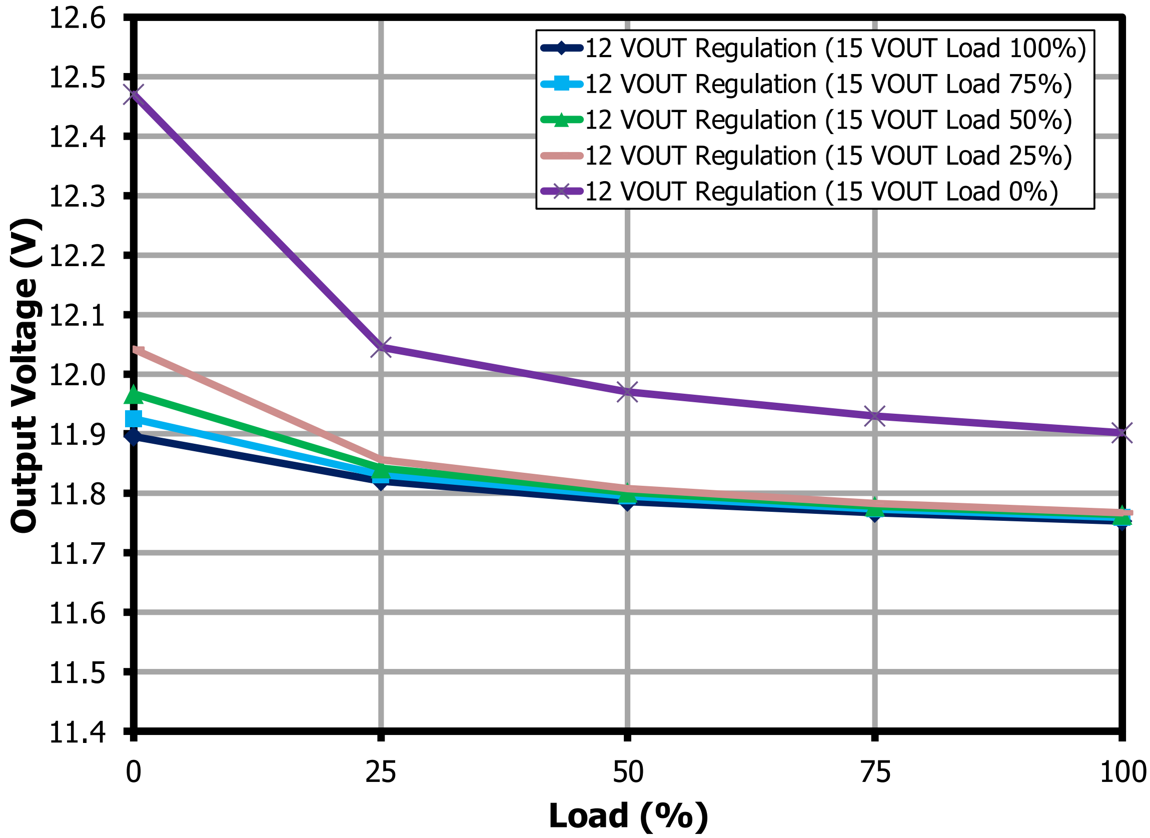

Figure 18 – Output Voltage vs. Percent Load.

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10.5.8 Cross Regulation 12 V at 265 VAC

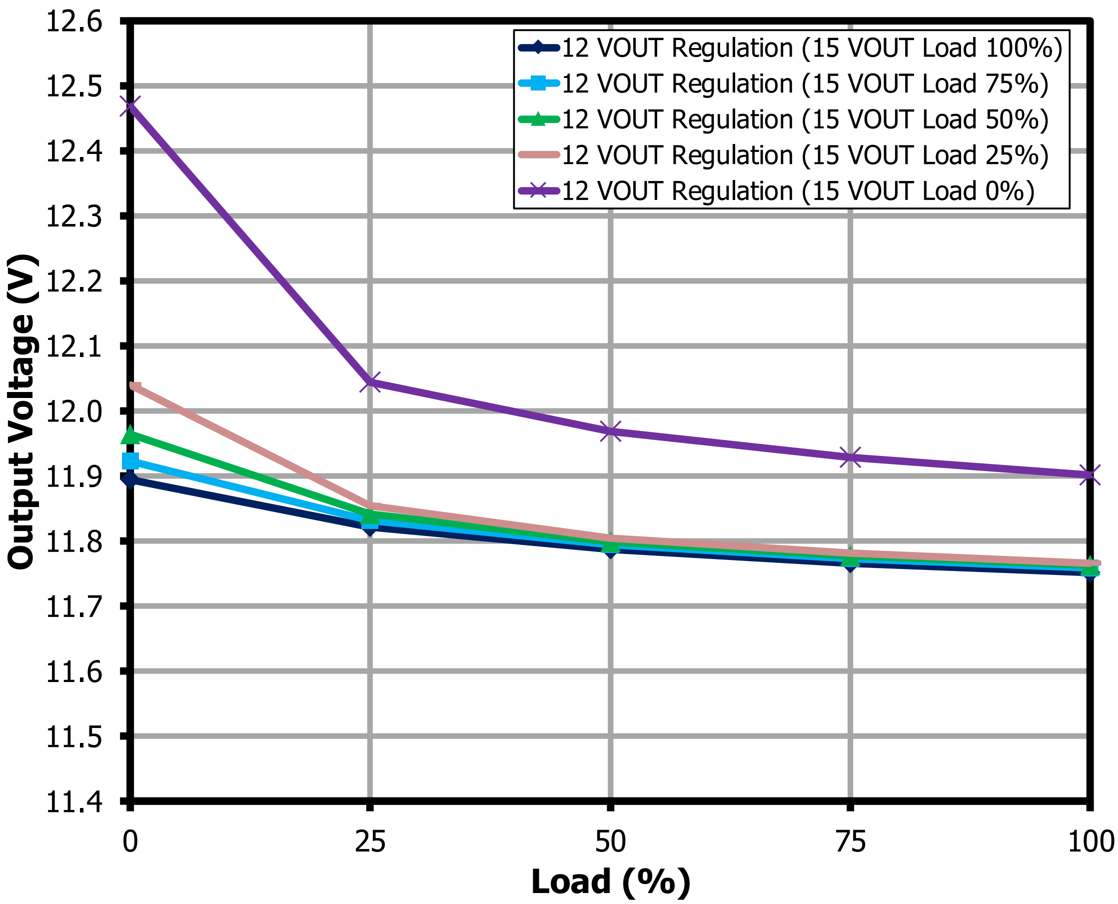

Figure 19 – Output Voltage vs. Percent Load.

11 Waveforms

11.1 *Load Transient Response*

Test Condition: Dynamic load frequency = 100 Hz, Duty cycle = 50 %
Slew Rate = 0.5 A / μs

11.1.1 12 V Transient 10% - 100% Load Change (15 V at 100% Load)

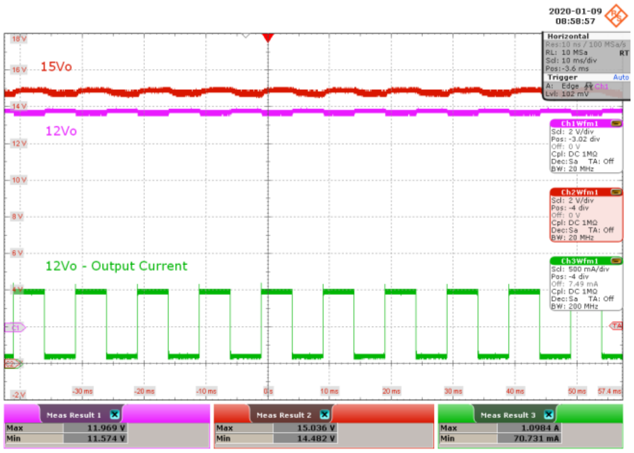

Figure 20 – 90 VAC 60 Hz.
CH1: V_{12V_OUT}, 2 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 2 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 500 mA / div., 10 ms / div.
12 V_{OUT}: V_{MAX}: 11.969 V, V_{MIN}: 11.574 V.
15 V_{OUT}: V_{MAX}: 15.036 V, V_{MIN}: 14.482 V.

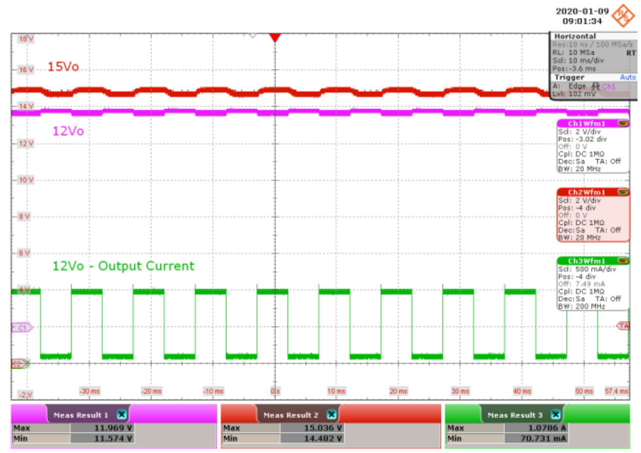

Figure 21 – 115 VAC 60 Hz.
CH1: V_{12V_OUT}, 2 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 2 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 500 mA / div., 10 ms / div.
12 V_{OUT}: V_{MAX}: 11.969 V, V_{MIN}: 11.574 V.
15 V_{OUT}: V_{MAX}: 15.036 V, V_{MIN}: 14.482 V.

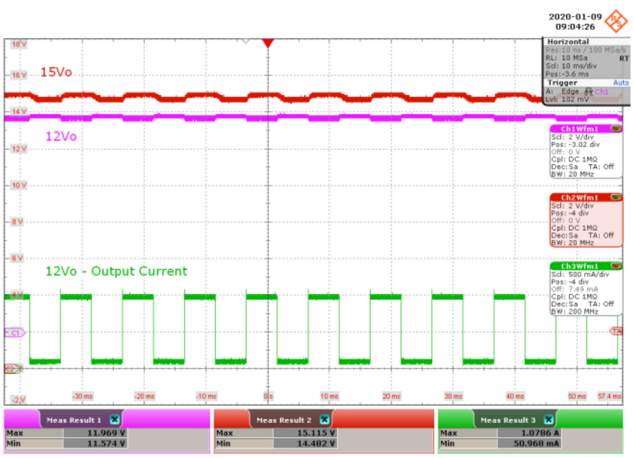

Figure 22 – 230 VAC 50 Hz.
CH1: V_{12V_OUT}, 2 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 2 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 500 mA / div., 10 ms / div.
12 V_{OUT}: V_{MAX}: 11.969 V, V_{MIN}: 11.574 V.
15 V_{OUT}: V_{MAX}: 15.115 V, V_{MIN}: 14.482 V.

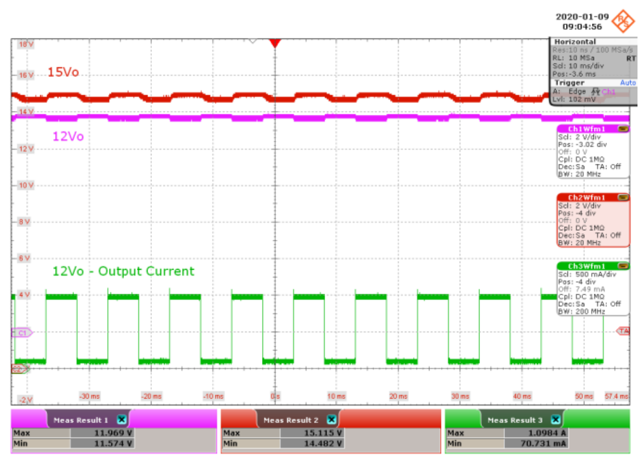

Figure 23 – 265 VAC 50 Hz.
CH1: V_{12V_OUT}, 2 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 2 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 500 mA / div., 10 ms / div.
12 V_{OUT}: V_{MAX}: 11.969 V, V_{MIN}: 11.574 V.
15 V_{OUT}: V_{MAX}: 15.115 V, V_{MIN}: 14.482 V.

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11.1.2 12 V Transient 50% - 100% Load Change (15 V at 100% Load)

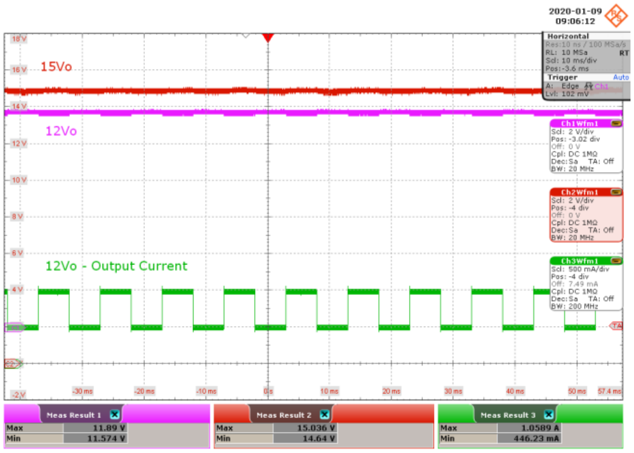

Figure 24 – 90 VAC 60 Hz.
CH1: V_{12V_OUT}, 2 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 2 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 500 mA / div., 10 ms / div..
12 V_{OUT}: V_{MAX}: 11.89 V, V_{MIN}: 11.574 V.
15 V_{OUT}: V_{MAX}: 15.036 V, V_{MIN}: 14.64 V.

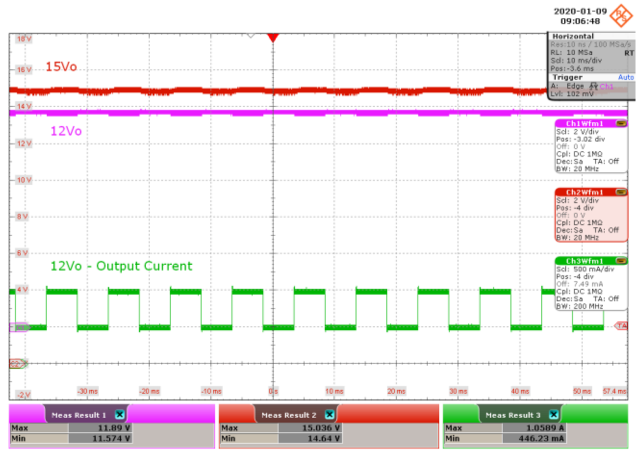

Figure 25 – 115 VAC 60 Hz.
CH1: V_{12V_OUT}, 2 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 2 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 500 mA / div., 10 ms / div.
12 V_{OUT}: V_{MAX}: 11.89 V, V_{MIN}: 11.574 V.
15 V_{OUT}: V_{MAX}: 15.036 V, V_{MIN}: 14.64 V.

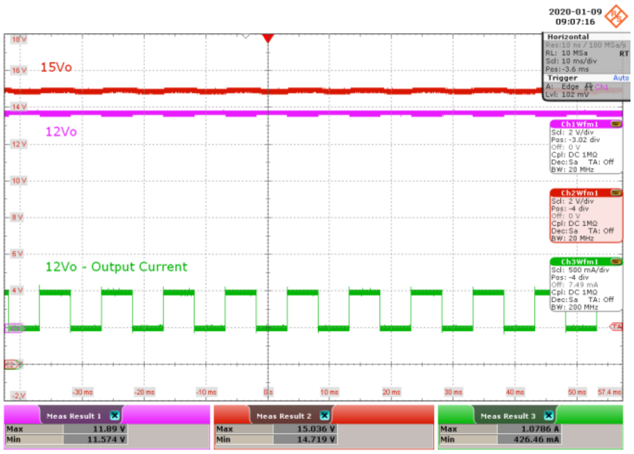

Figure 26 – 230 VAC 50 Hz.
CH1: V_{12V_OUT}, 2 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 2 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 500 mA / div., 10 ms / div.
12 V_{OUT}: V_{MAX}: 11.89 V, V_{MIN}: 11.574 V.
15 V_{OUT}: V_{MAX}: 15.036 V, V_{MIN}: 14.719 V.

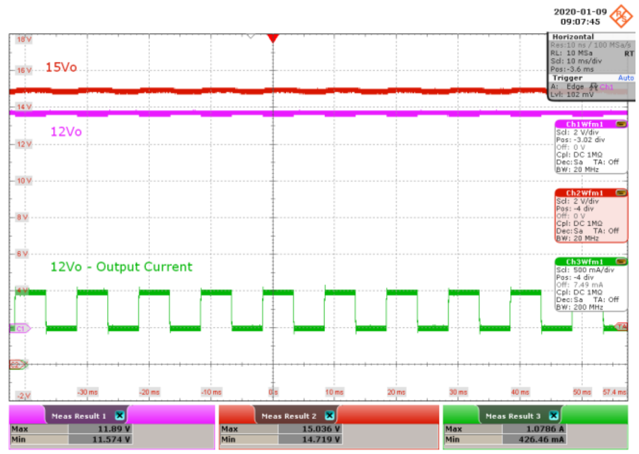

Figure 27 – 265 VAC 50 Hz.
CH1: V_{12V_OUT}, 2 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 2 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 500 mA / div., 10 ms / div.
12 V_{OUT}: V_{MAX}: 11.89 V, V_{MIN}: 11.574 V.
15 V_{OUT}: V_{MAX}: 15.036 V, V_{MIN}: 14.719 V.

11.1.3 15 V Transient 10% - 100% Load Change (12 V at 100% Load)

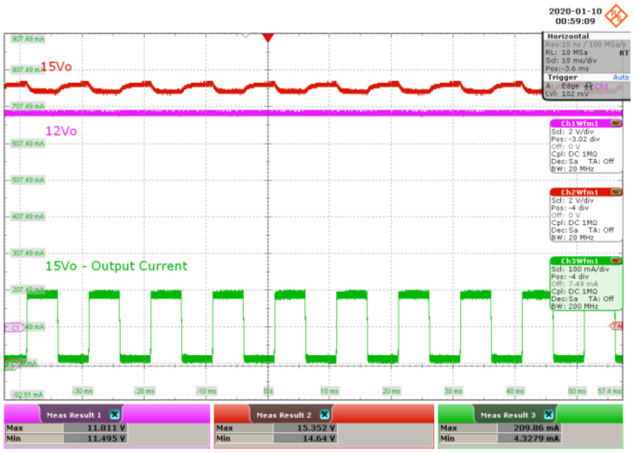

Figure 28 – 90 VAC 60 Hz.
CH1: V_{12V_OUT}, 2 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 2 V / div., 10 ms / div.
CH3: I_{15V_OUT}, 100 mA / div., 10 ms / div.
12 V_{OUT}: V_{MAX}: 11.811 V, V_{MIN}: 11.495 V.
15 V_{OUT}: V_{MAX}: 15.352 V, V_{MIN}: 14.64 V.

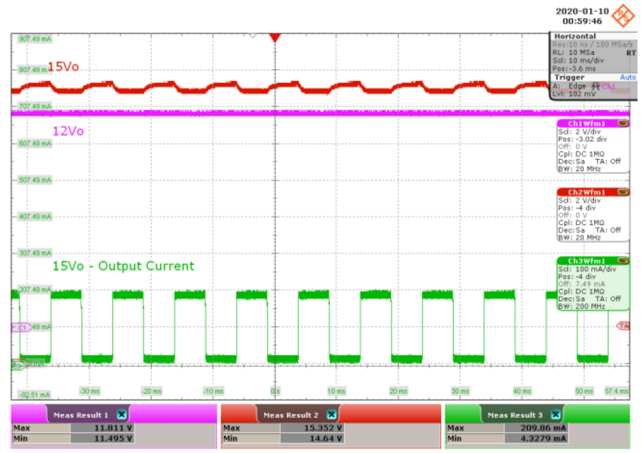

Figure 29 – 115 VAC 60 Hz.
CH1: V_{12V_OUT}, 2 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 2 V / div., 10 ms / div.
CH3: I_{15V_OUT}, 100 mA / div., 10 ms / div.
12 V_{OUT}: V_{MAX}: 11.811 V, V_{MIN}: 11.495 V.
15 V_{OUT}: V_{MAX}: 15.352 V, V_{MIN}: 14.64 V.

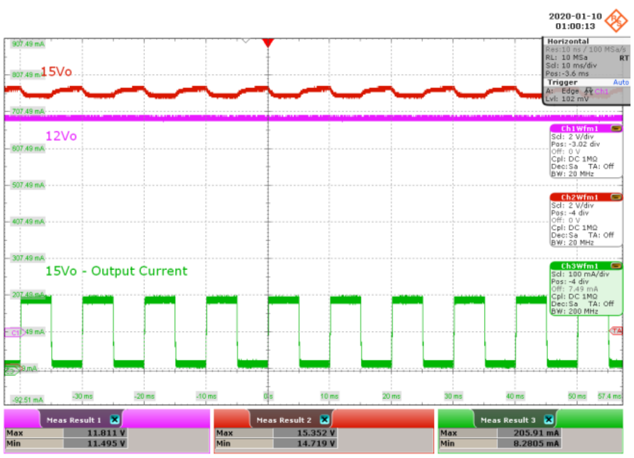

Figure 30 – 230 VAC 50 Hz.
CH1: V_{12V_OUT}, 2 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 2 V / div., 10 ms / div.
CH3: I_{15V_OUT}, 100 mA / div., 10 ms / div.
12 V_{OUT}: V_{MAX}: 11.811 V, V_{MIN}: 11.495 V.
15 V_{OUT}: V_{MAX}: 15.352 V, V_{MIN}: 14.719 V.

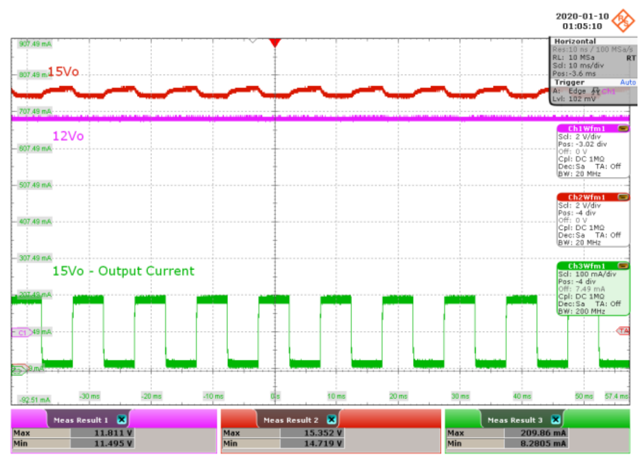

Figure 31 – 265 VAC 50 Hz.
CH1: V_{12V_OUT}, 2 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 2 V / div., 10 ms / div.
CH3: I_{15V_OUT}, 100 mA / div., 10 ms / div.
12 V_{OUT}: V_{MAX}: 11.811 V, V_{MIN}: 11.495 V.
15 V_{OUT}: V_{MAX}: 15.352 V, V_{MIN}: 14.719 V.

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11.1.4 15 V Transient 50% - 100% Load Change (12 V at 100% Load)

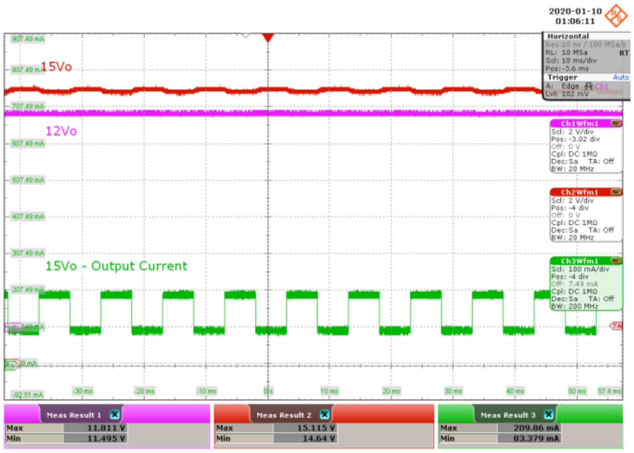

Figure 32 – 90 VAC 60 Hz.
CH1: V_{12V_OUT}, 2 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 2 V / div., 10 ms / div.
CH3: I_{15V_OUT}, 100 mA / div., 10 ms / div.
12 V_{OUT}: V_{MAX}: 11.811 V, V_{MIN}: 11.495 V.
15 V_{OUT}: V_{MAX}: 15.115 V, V_{MIN}: 14.64 V.

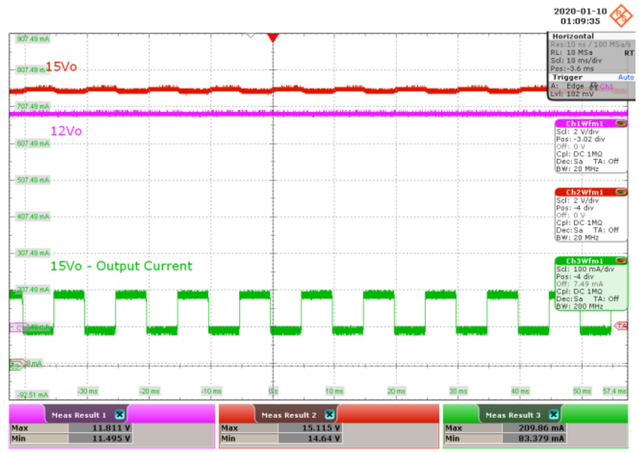

Figure 33 – 115 VAC 60 Hz.
CH1: V_{12V_OUT}, 2 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 2 V / div., 10 ms / div.
CH3: I_{15V_OUT}, 100 mA / div., 10 ms / div.
12 V_{OUT}: V_{MAX}: 11.811 V, V_{MIN}: 11.495 V.
15 V_{OUT}: V_{MAX}: 15.115 V, V_{MIN}: 14.64 V.

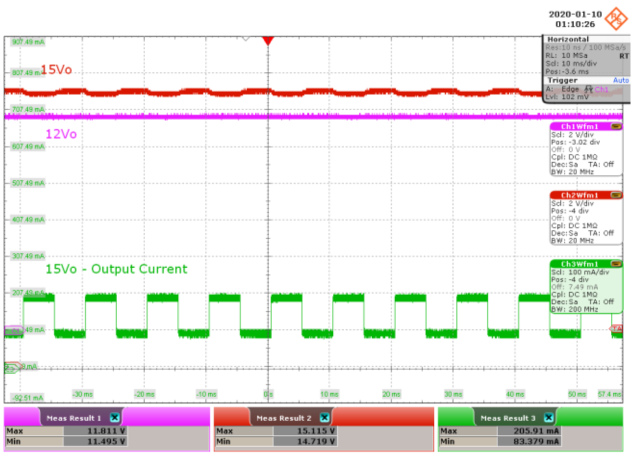

Figure 34 – 230 VAC 50 Hz.
CH1: V_{12V_OUT}, 2 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 2 V / div., 10 ms / div.
CH3: I_{15V_OUT}, 100 mA / div., 10 ms / div.
12 V_{OUT}: V_{MAX}: 11.811 V, V_{MIN}: 11.495 V.
15 V_{OUT}: V_{MAX}: 15.115 V, V_{MIN}: 14.719 V.

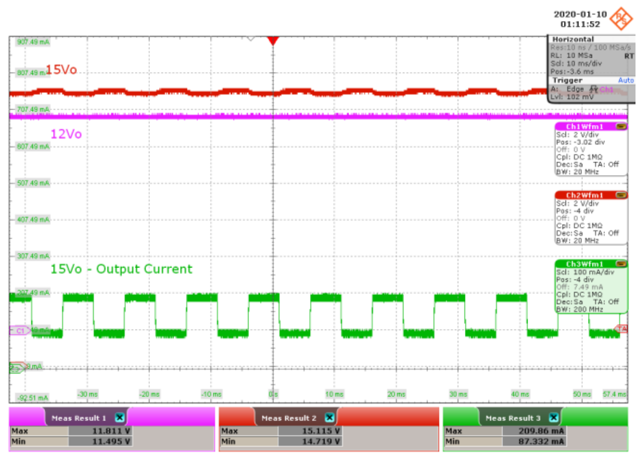

Figure 35 – 265 VAC 50 Hz.
CH1: V_{12V_OUT}, 2 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 2 V / div., 10 ms / div.
CH3: I_{15V_OUT}, 100 mA / div., 10 ms / div.
12 V_{OUT}: V_{MAX}: 11.811 V, V_{MIN}: 11.495 V.
15 V_{OUT}: V_{MAX}: 15.115 V, V_{MIN}: 14.719 V.

11.2 ***Output Voltage at Start-up***

11.2.1 Full Load CC Mode

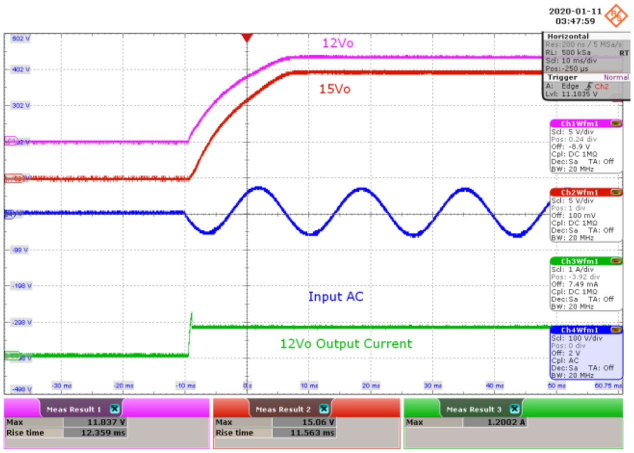

Figure 36 – 90 VAC 60 Hz.
CH1: V_{12V_OUT}, 5 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 5 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 1 A / div., 10 ms / div.
CH4: V_{in}, 100 V / div., 10 ms / div.
Rise Time: V_{12V} = 13 ms., V_{15V} = 12 ms.
V_{MAX}: V_{12V} = 11.83 V, V_{15V} = 15.06 V.

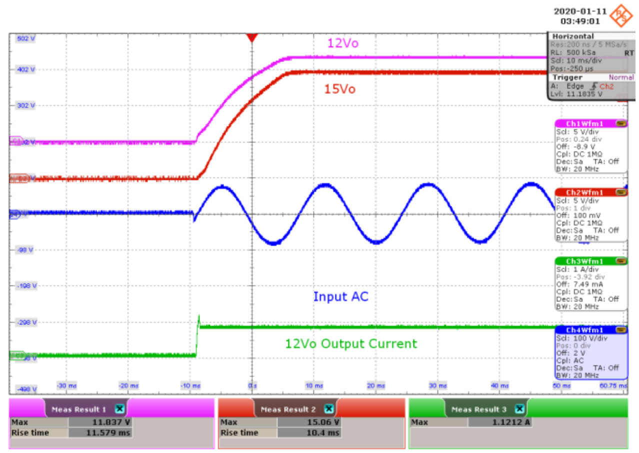

Figure 37 – 115 VAC 60 Hz.
CH1: V_{12V_OUT}, 5 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 5 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 1 A / div., 10 ms / div.
CH4: V_{in}, 100 V / div., 10 ms / div.
Rise Time: V_{12V} = 12 ms., V_{15V} = 11 ms.
V_{MAX}: V_{12V} = 11.83 V, V_{15V} = 15.06 V.

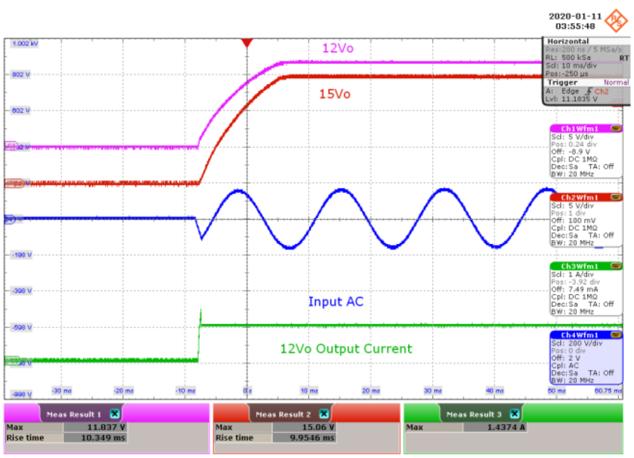

Figure 38 – 230 VAC 50 Hz.
CH1: V_{12V_OUT}, 5 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 5 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 1 A / div., 10 ms / div.
CH4: V_{in}, 200 V / div., 10 ms / div.
Rise Time: V_{12V} = 11 ms., V_{15V} = 10 ms.
V_{MAX}: V_{12V} = 11.83 V, V_{15V} = 15.06 V.

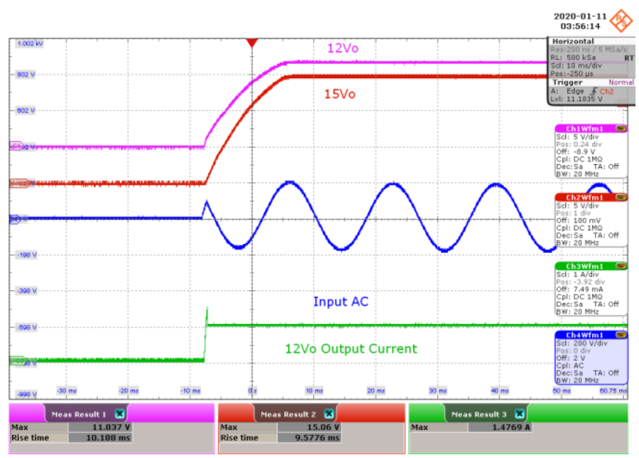

Figure 39 – 265 VAC 50 Hz.
CH1: V_{12V_OUT}, 5 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 5 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 1 A / div., 10 ms / div.
CH4: V_{in}, 200 V / div., 10 ms / div
Rise Time: V_{12V} = 11 ms., V_{15V} = 10 ms.
V_{MAX}: V_{12V} = 11.83 V, V_{15V} = 15.06 V.

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11.2.2 Full Load CR Mode

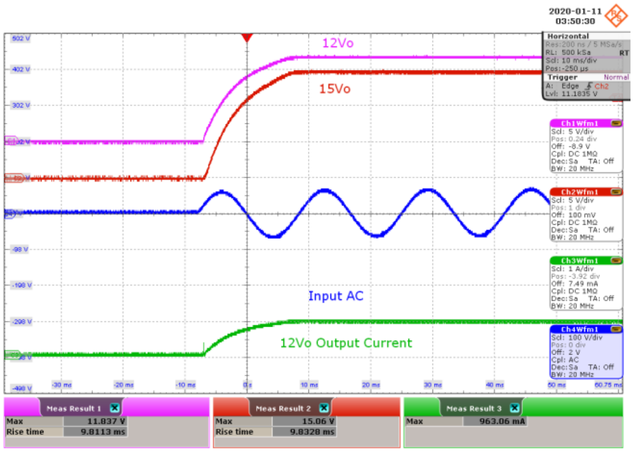

Figure 40 – 90 VAC 60 Hz.
CH1: V_{12V_OUT}, 5 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 5 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 1 A / div., 10 ms / div.
CH4: V_{in}, 100 V / div., 10 ms / div.
Rise Time: V_{12V} = 10 ms., V_{15V} = 10 ms.
V_{MAX}: V_{12V} = 11.83 V, V_{15V} = 15.06 V.

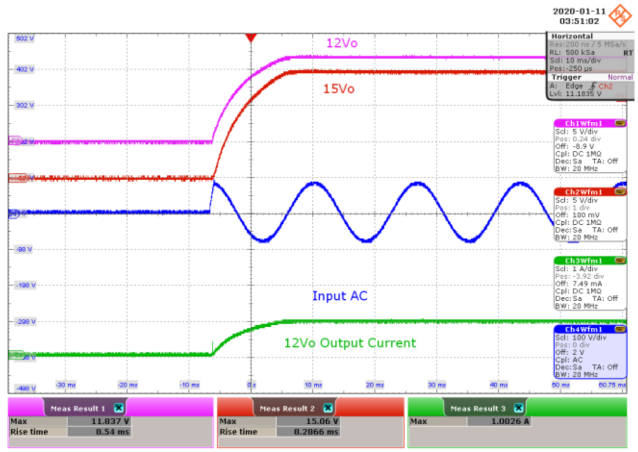

Figure 41 – 115 VAC 60 Hz.
CH1: V_{12V_OUT}, 5 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 5 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 1 A / div., 10 ms / div.
CH4: V_{in}, 100 V / div., 10 ms / div.
Rise Time: V_{12V} = 9 ms., V_{15V} = 9 ms.
V_{MAX}: V_{12V} = 11.83 V, V_{15V} = 15.06 V.

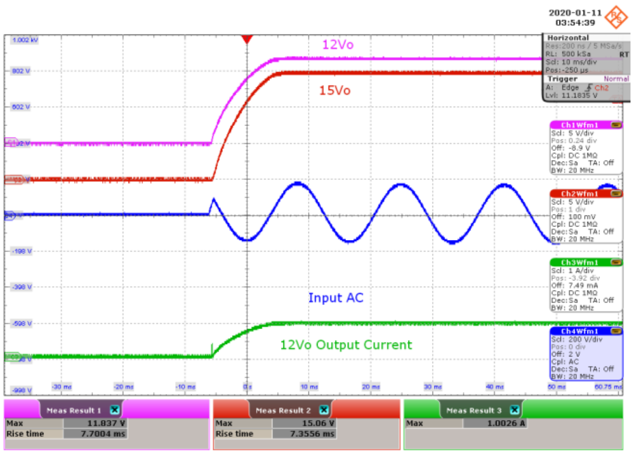

Figure 42 – 230 VAC 50 Hz.
CH1: V_{12V_OUT}, 5 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 5 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 1 A / div., 10 ms / div.
CH4: V_{in}, 200 V / div., 10 ms / div.
Rise Time: V_{12V} = 8 ms., V_{15V} = 8 ms.
V_{MAX}: V_{12V} = 11.83 V, V_{15V} = 15.06 V.

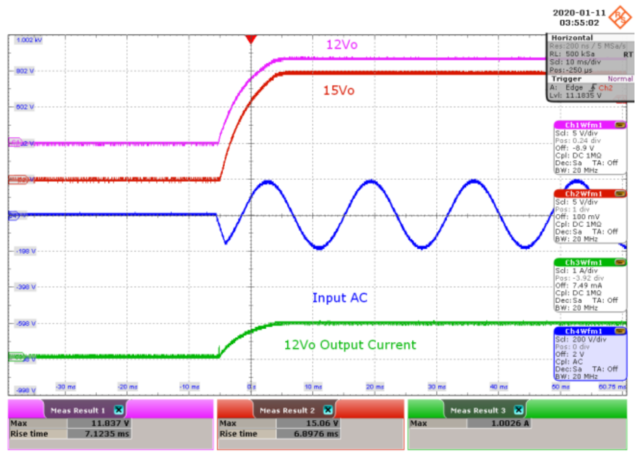

Figure 43 – 265 VAC 50 Hz.
CH1: V_{12V_OUT}, 5 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 5 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 1 A / div., 10 ms / div.
CH4: V_{in}, 200 V / div., 10 ms / div
Rise Time: V_{12V} = 8 ms., V_{15V} = 7 ms.
V_{MAX}: V_{12V} = 11.83 V, V_{15V} = 15.06 V.

11.2.3 0% Load

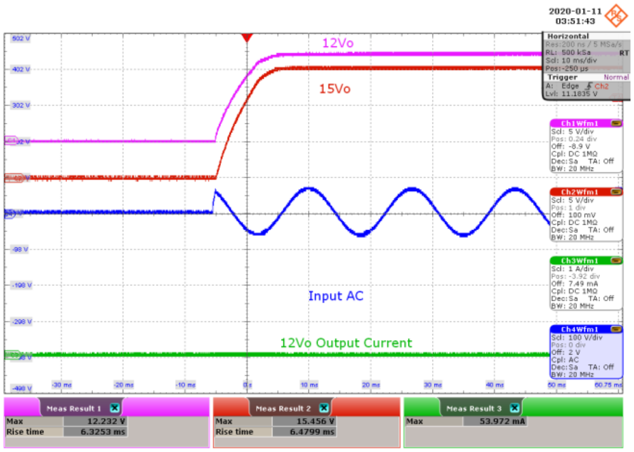

Figure 44 – 90 VAC 60 Hz.
CH1: V_{12V_OUT}, 5 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 5 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 1 A / div., 10 ms / div.
CH4: V_{in}, 100 V / div., 10 ms / div.
Rise Time: V_{12V} = 7 ms., V_{15V} = 7 ms.
V_{MAX}: V_{12V} = 12.23 V, V_{15V} = 15.45 V.

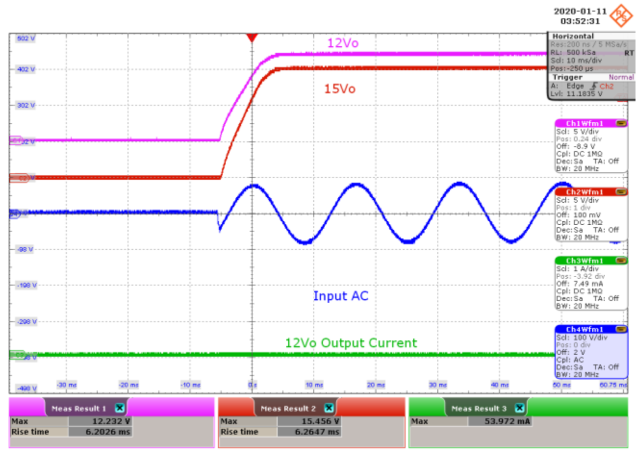

Figure 45 – 90 VAC 60 Hz.
CH1: V_{12V_OUT}, 5 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 5 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 1 A / div., 10 ms / div.
CH4: V_{in}, 100 V / div., 10 ms / div.
Rise Time: V_{12V} = 7 ms., V_{15V} = 7 ms.
V_{MAX}: V_{12V} = 12.23 V, V_{15V} = 15.45 V.

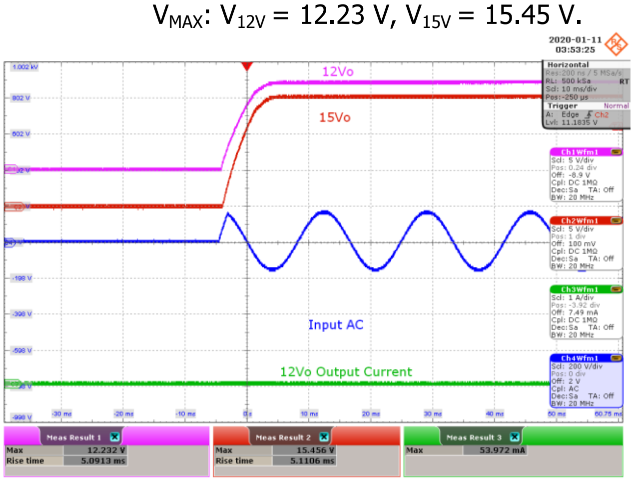

Figure 46 – 230 VAC 50 Hz.
CH1: V_{12V_OUT}, 5 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 5 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 1 A / div., 10 ms / div.
CH4: V_{in}, 200 V / div., 10 ms / div.
Rise Time: V_{12V} = 6 ms., V_{15V} = 6 ms.
V_{MAX}: V_{12V} = 12.23 V, V_{15V} = 15.45 V.

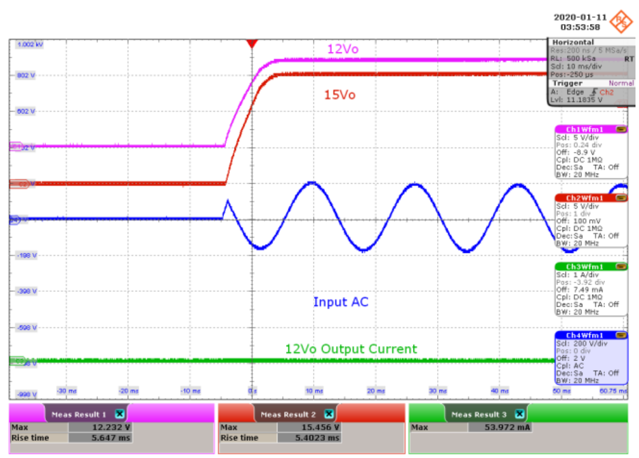

Figure 47 – 230 VAC 50 Hz.
CH1: V_{12V_OUT}, 5 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 5 V / div., 10 ms / div.
CH3: I_{12V_OUT}, 1 A / div., 10 ms / div.
CH4: V_{in}, 200 V / div., 10 ms / div.
Rise Time: V_{12V} = 6 ms., V_{15V} = 6 ms.
V_{MAX}: V_{12V} = 12.23 V, V_{15V} = 15.45 V.

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11.3 ***Switching Waveforms***

11.3.1 Primary MOSFET Drain-Source Voltage and Current at Normal Operation

11.3.1.1 100% Load

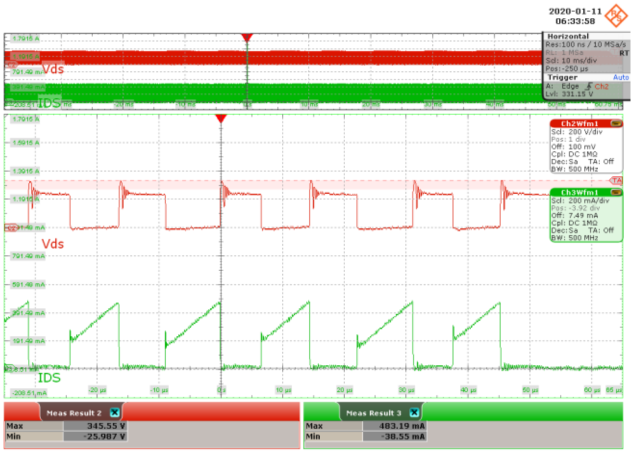

Figure 48 – 90 VAC 60 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 345.55 V, $I_{DS(MAX)}$ = 0.483 A.

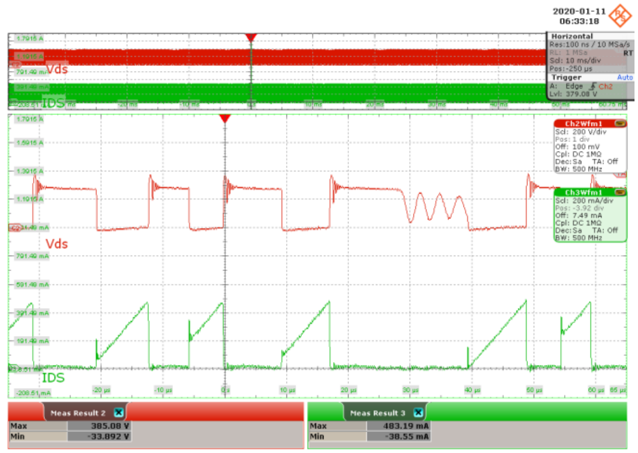

Figure 49 – 115 VAC 60 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 385.08 V, $I_{DS(MAX)}$ = 0.483 A.

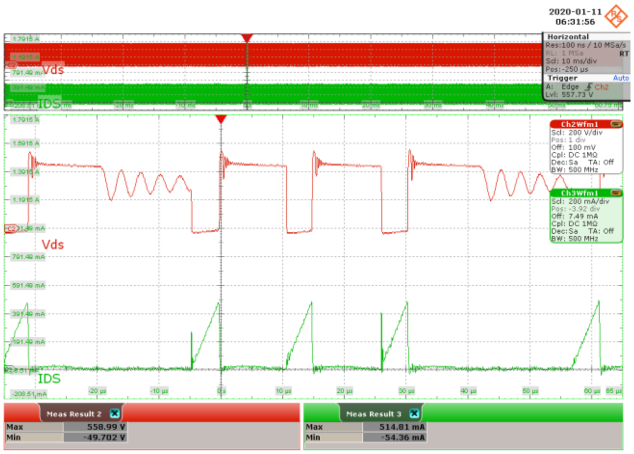

Figure 50 – 230 VAC 50 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 558.99 V, $I_{DS(MAX)}$ = 0.514 A.

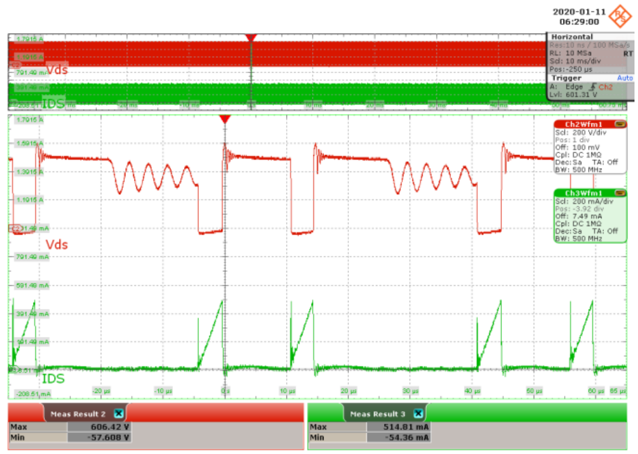

Figure 51 – 265 VAC 50 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 606.42 V, $I_{DS(MAX)}$ = 0.514 A.

11.3.1.2 0% Load

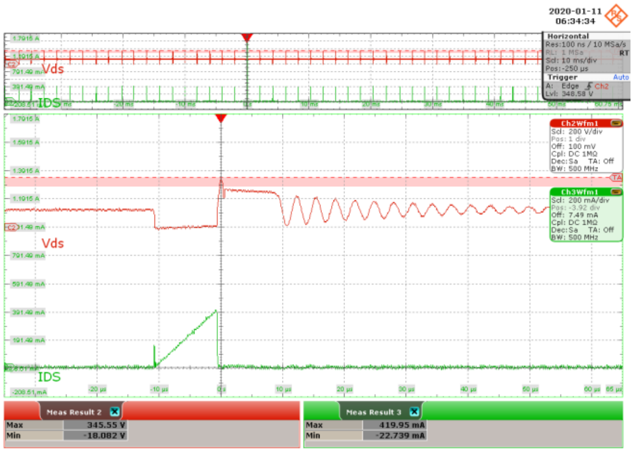

Figure 52 – 90 VAC 60 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 345.55 V, $I_{DS(MAX)}$ = 0.419 A.

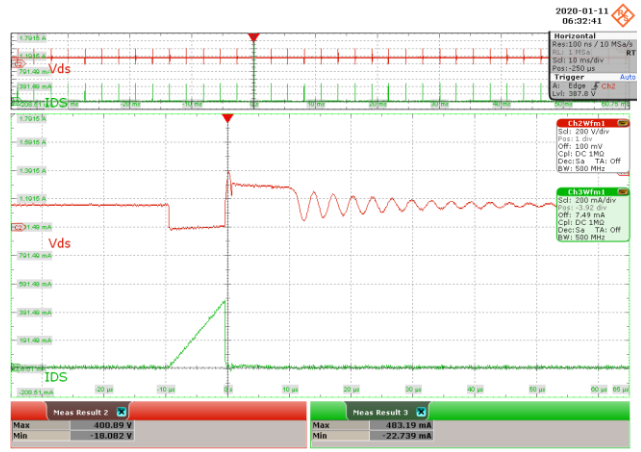

Figure 53 – 115 VAC 60 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 400.89 V, $I_{DS(MAX)}$ = 0.483 A.

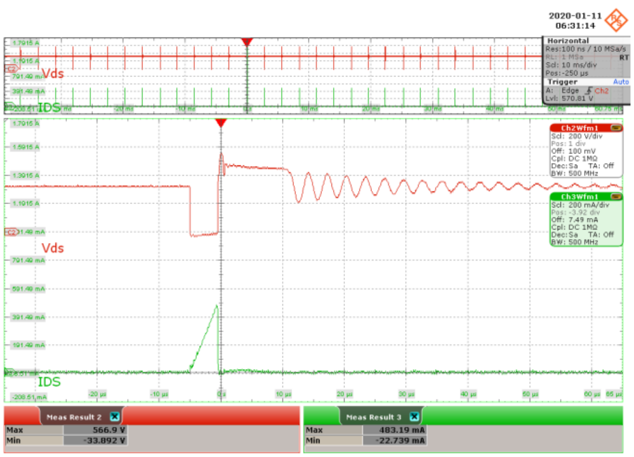

Figure 54 – 230 VAC 50 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 566.9 V, $I_{DS(MAX)}$ = 0.483 A.

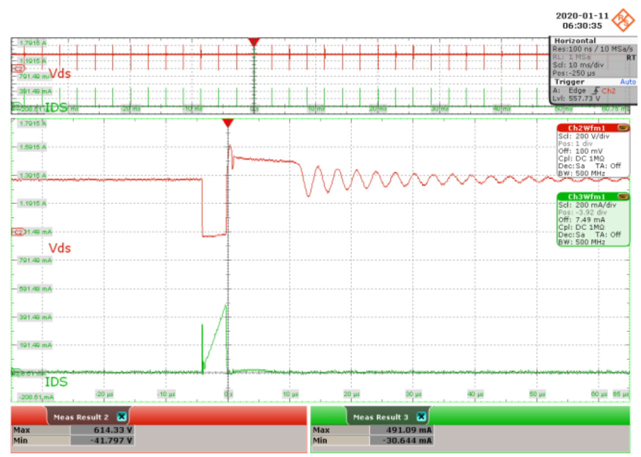

Figure 55 – 265 VAC 50 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 614.33 V, $I_{DS(MAX)}$ = 0.491 A.

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11.3.2 Primary MOSFET Drain-Source Voltage and Current at Start-up Operation

11.3.2.1 100% Load

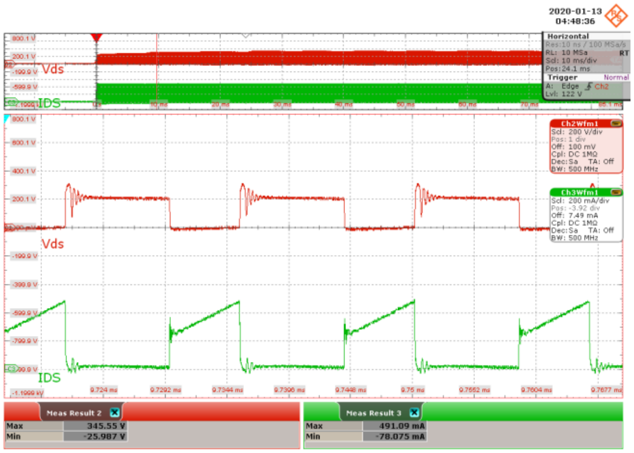

Figure 56 – 90 VAC 60 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 5.2 μs / div.
$V_{DS(MAX)}$ = 345.55 V, $I_{DS(MAX)}$ = 0.491 A.

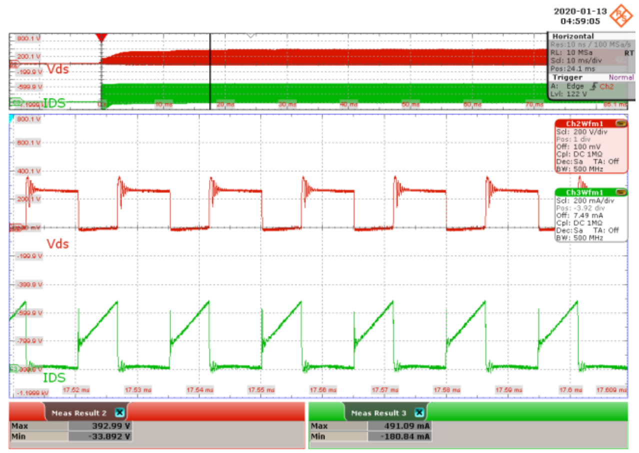

Figure 57 – 115 VAC 60 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 μs / div.
$V_{DS(MAX)}$ = 392.99 V, $I_{DS(MAX)}$ = 0.491 A.

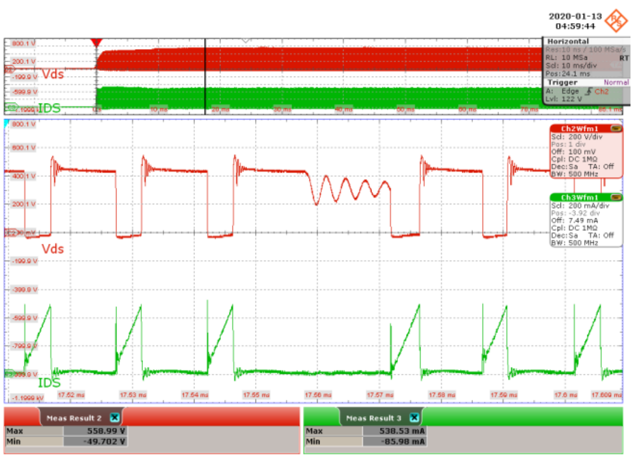

Figure 58 – 230 VAC 50 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 μs / div.
$V_{DS(MAX)}$ = 558.99 V, $I_{DS(MAX)}$ = 0.538 A.

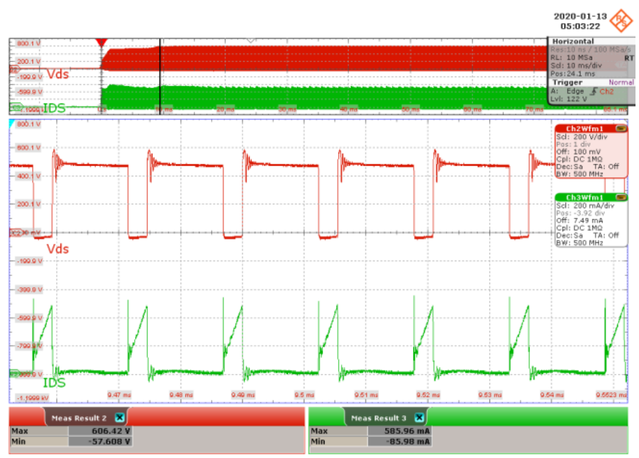

Figure 59 – 265 VAC 50 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 μs / div.
$V_{DS(MAX)}$ = 606.42 V, $I_{DS(MAX)}$ = 0.585 A.

11.3.2.2 0% Load

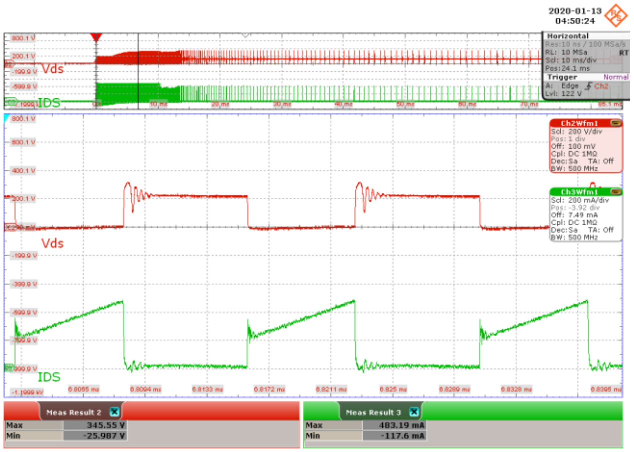

Figure 60 – 90 VAC 60 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 3.9 µs / div.
$V_{DS(MAX)}$ = 345.55 V, $I_{DS(MAX)}$ = 0.483 A.

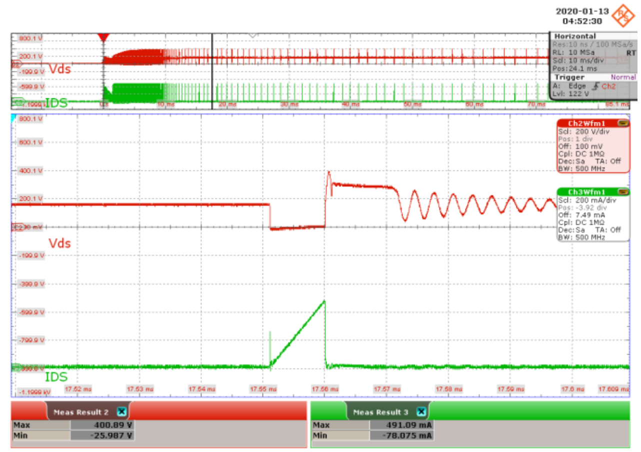

Figure 61 – 115 VAC 60 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 400.89 V, $I_{DS(MAX)}$ = 0.491 A.

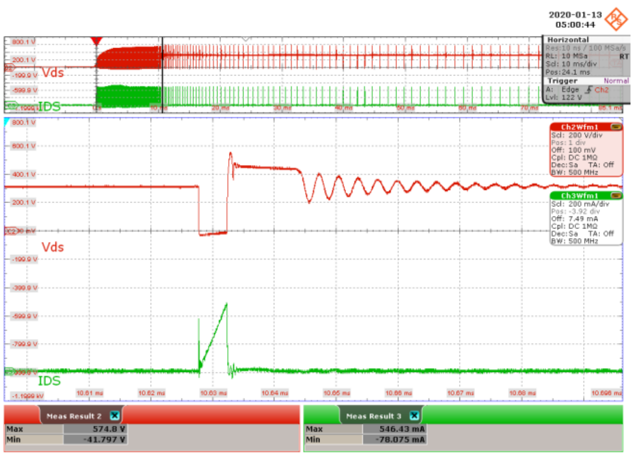

Figure 62 – 230 VAC 50 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 574.8 V, $I_{DS(MAX)}$ = 0.546 A.

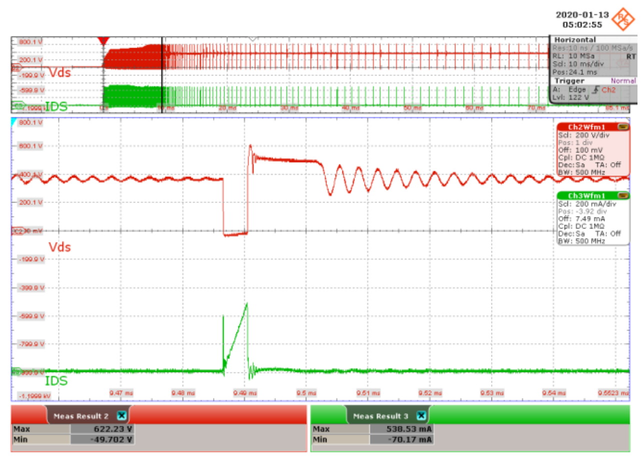

Figure 63 – 265 VAC 50 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 622.23 V, $I_{DS(MAX)}$ = 0.538 A.

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11.3.3 Free Wheeling Diode Voltage and Current at Normal Operation

11.3.3.1 100% Load

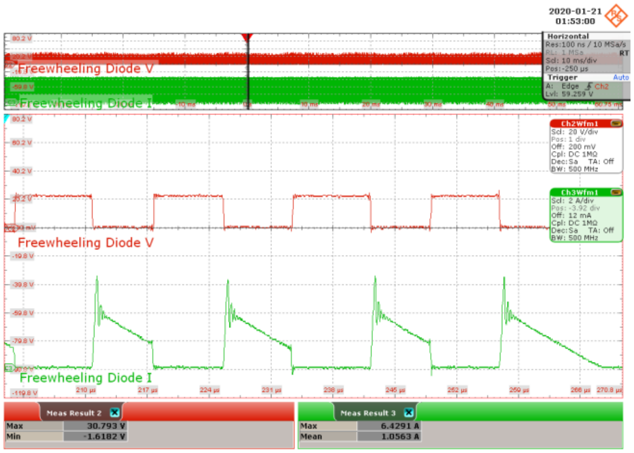

Figure 64 – 90 VAC 60 Hz.
CH2: V_{DIODE}, 20 V / div., 10 ms / div.
CH3: I_{DIODE}, 2 A / div., 10 ms / div.
Zoom: 7 µs / div.
PIV = 30.793 V, $I_{D(MEAN)}$ = 1.0563 A.

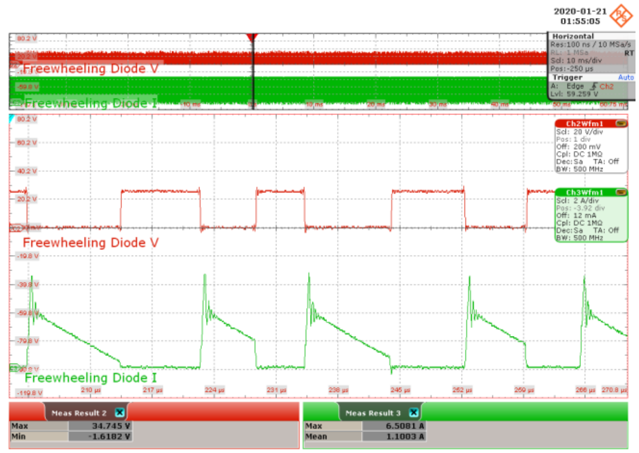

Figure 65 – 115 VAC 60 Hz.
CH2: V_{DIODE}, 20 V / div., 10 ms / div.
CH3: I_{DIODE}, 2 A / div., 10 ms / div.
Zoom: 7 µs / div.
PIV = 34.745 V, $I_{D(MEAN)}$ = 1.1003 A.

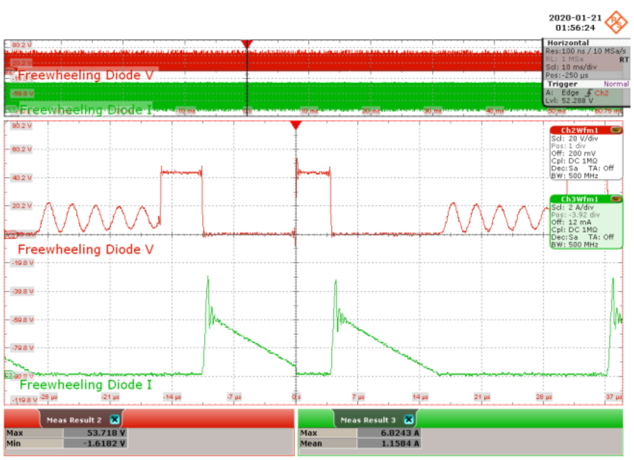

Figure 66 – 230 VAC 50 Hz.
CH2: V_{DIODE}, 20 V / div., 10 ms / div.
CH3: I_{DIODE}, 2 A / div., 10 ms / div.
Zoom: 7 µs / div.
PIV = 53.718 V, $I_{D(MEAN)}$ = 1.1584 A.

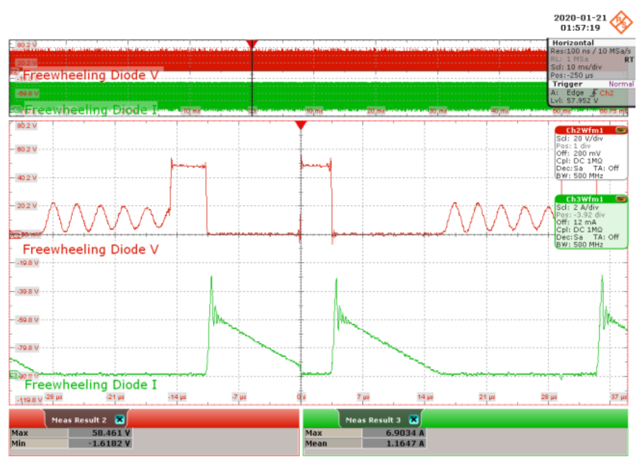

Figure 67 – 265 VAC 50 Hz.
CH2: V_{DIODE}, 20 V / div., 10 ms / div.
CH3: I_{DIODE}, 2 A / div., 10 ms / div.
Zoom: 7 µs / div.
PIV = 58.461 V, $I_{D(MEAN)}$ = 1.1647 A.

11.3.3.2 0% Load

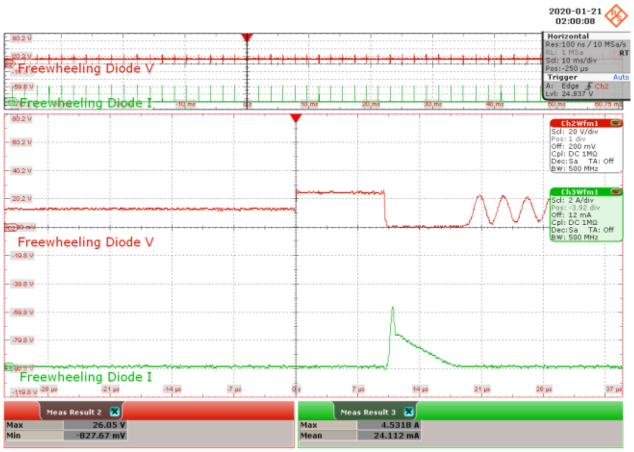

Figure 68 – 90 VAC 60 Hz.
CH2: V_{DIODE}, 20 V / div., 10 ms / div.
CH3: I_{DIODE}, 2 A / div., 10 ms / div.
Zoom: 7 µs / div.
PIV = 26.05 V, $I_{D(MEAN)}$ = 24.11 mA.

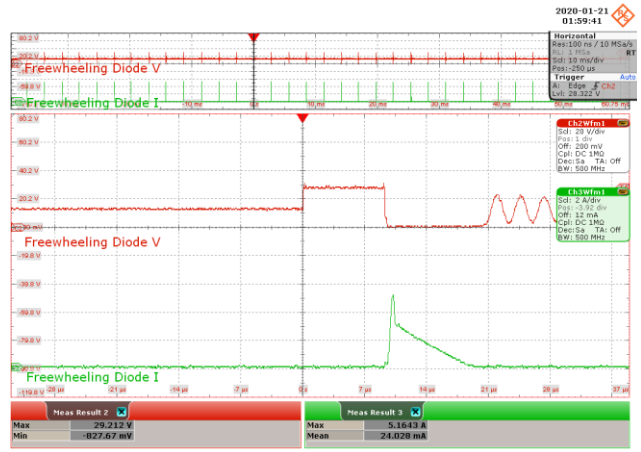

Figure 69 – 115 VAC 60 Hz.
CH2: V_{DIODE}, 20 V / div., 10 ms / div.
CH3: I_{DIODE}, 2 A / div., 10 ms / div.
Zoom: 7 µs / div.
PIV = 29.212 V, $I_{D(MEAN)}$ = 24.028 mA.

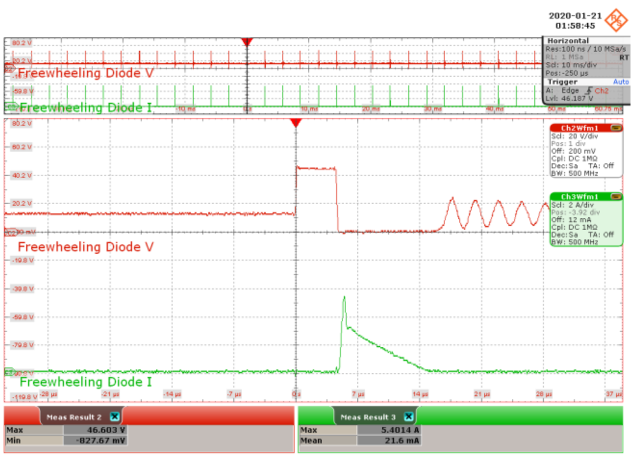

Figure 70 – 230 VAC 50 Hz.
CH2: V_{DIODE}, 20 V / div., 10 ms / div.
CH3: I_{DIODE}, 2 A / div., 10 ms / div.
Zoom: 7 µs / div.
PIV = 46.603 V, $I_{D(MEAN)}$ = 21.6 mA.

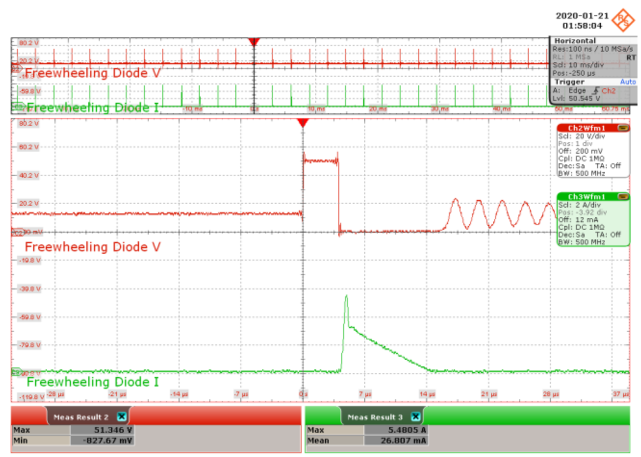

Figure 71 – 265 VAC 50 Hz.
CH2: V_{DIODE}, 20 V / div., 10 ms / div.
CH3: I_{DIODE}, 2 A / div., 10 ms / div.
Zoom: 7 µs / div.
PIV = 51.346 V, $I_{D(MEAN)}$ = 26.807 mA.

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11.4 ***Fault Conditions***

11.4.1 12 V Output Short-Circuit at Normal Operation

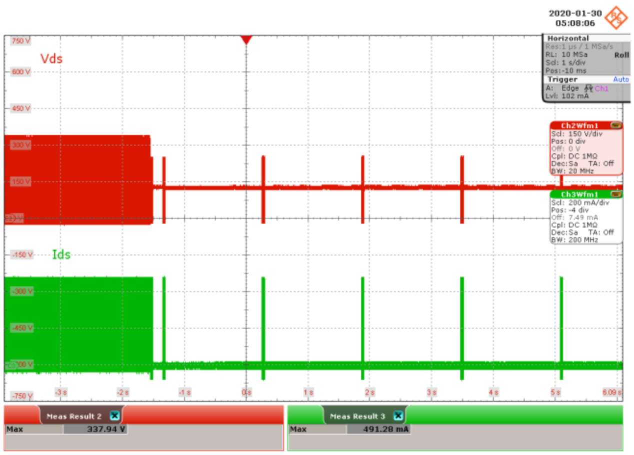

Figure 72 – 90 VAC 60 Hz. Output Short.
CH2: V_{DS}, 150 V / div., 1 s / div.
CH3: I_{DS}, 200 mA / div., 1 s / div.
$V_{DS(MAX)}$ = 337.94 V.
$I_{DS(MAX)}$ = 491.28 mA.

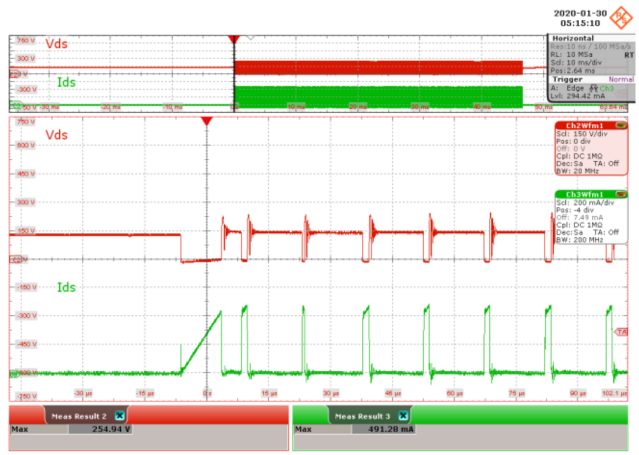

Figure 73 – 90 VAC 60 Hz. Auto Restart at Short.
CH2: V_{DS}, 150 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom 15 μs / div.
$V_{DS(MAX)}$ = 254.94 V.
$I_{DS(MAX)}$ = 491.28 mA.

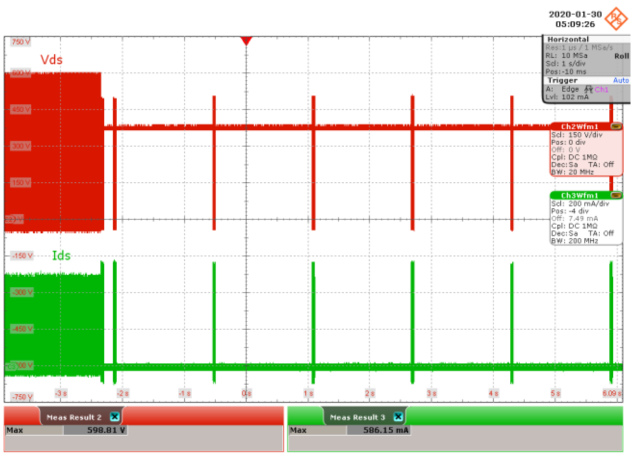

Figure 74 – 265 VAC 60 Hz. Output Short.
CH2: V_{DS}, 150 V / div., 1 s / div.
CH3: I_{DS}, 200 mA / div., 1 s / div.
$V_{DS(MAX)}$ = 598.81 V.
$I_{DS(MAX)}$ = 586.15 mA.

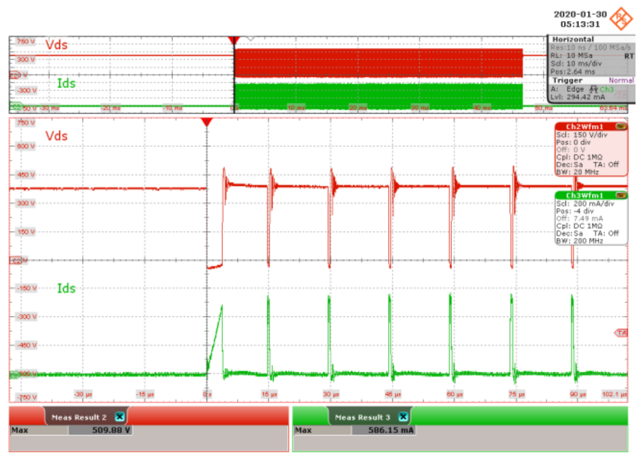

Figure 75 – 265 VAC 60 Hz. Auto Restart at Short.
CH2: V_{DS}, 150 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom 15 μs / div.
$V_{DS(MAX)}$ = 509.88 V.
$I_{DS(MAX)}$ = 586.15 mA.

11.4.1 15 V Output Short-Circuit

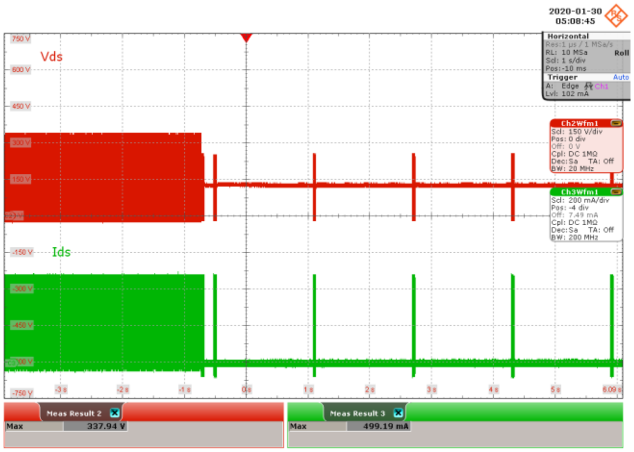

Figure 76 – 90 VAC 60 Hz. Output Short.
CH2: V_{DS}, 150 V / div., 1 s / div.
CH3: I_{DS}, 200 mA / div., 1 s / div.
$V_{DS(MAX)}$ = 337.94 V.
$I_{DS(MAX)}$ = 499.19 mA.

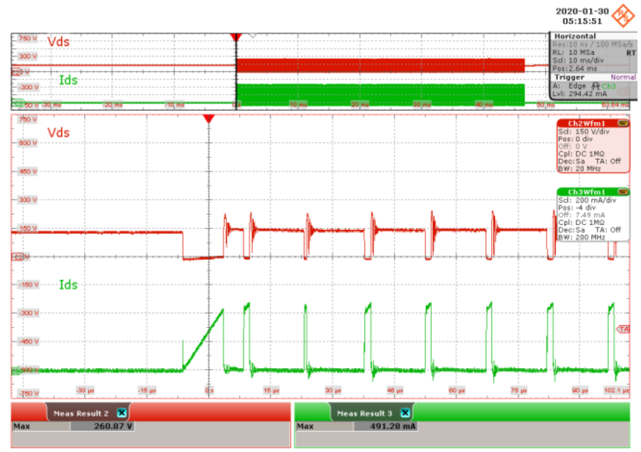

Figure 77 – 90 VAC 60 Hz. Auto Restart at Short.
CH2: V_{DS}, 150 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom 15 μs / div.
$V_{DS(MAX)}$ = 260.87 V.
$I_{DS(MAX)}$ = 491.28 mA.

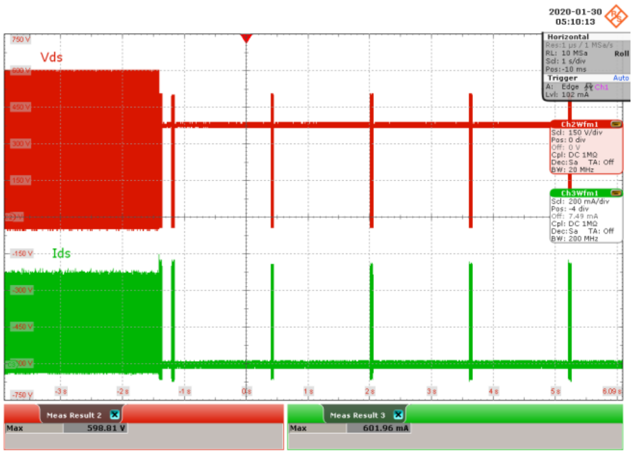

Figure 78 – 90 VAC 60 Hz. Output Short.
CH2: V_{DS}, 150 V / div., 1 s / div.
CH3: I_{DS}, 200 mA / div., 1 s / div.
$V_{DS(MAX)}$ = 598.81 V.
$I_{DS(MAX)}$ = 601.96 mA.

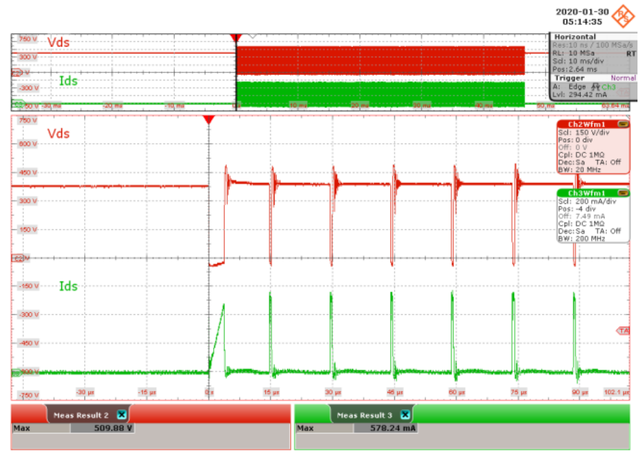

Figure 79 – 90 VAC 60 Hz. Auto Restart at Short.
CH2: V_{DS}, 150 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom 15 μs / div.
$V_{DS(MAX)}$ = 509.88 V.
$I_{DS(MAX)}$ = 578.24 mA.

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11.5 ***Output Voltage Ripple***

11.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

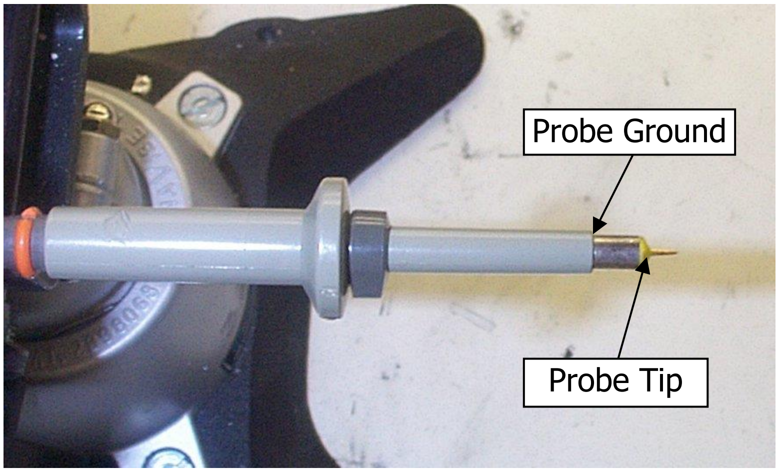

Figure 80 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

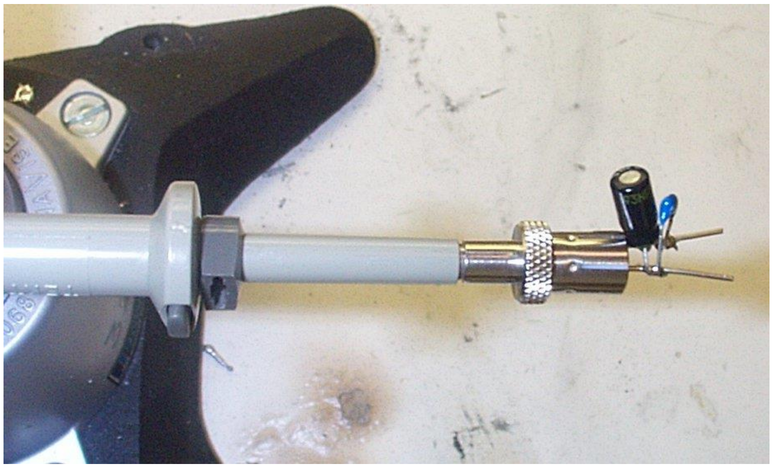

Figure 81 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

11.5.2 Measurement Results

Note: All ripple measurements were taken at PCB end.

11.5.2.1 100% Load Condition

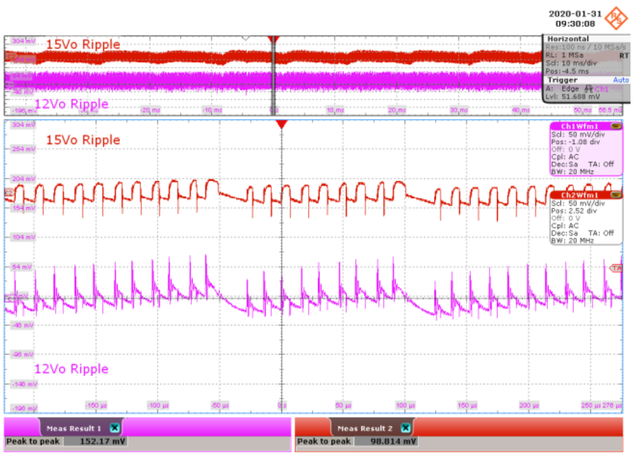

Figure 82 – 90 VAC 60 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 µs / div.
12 V Output Ripple = 152.17 mV.
15 V Output Ripple = 98.814 mV.

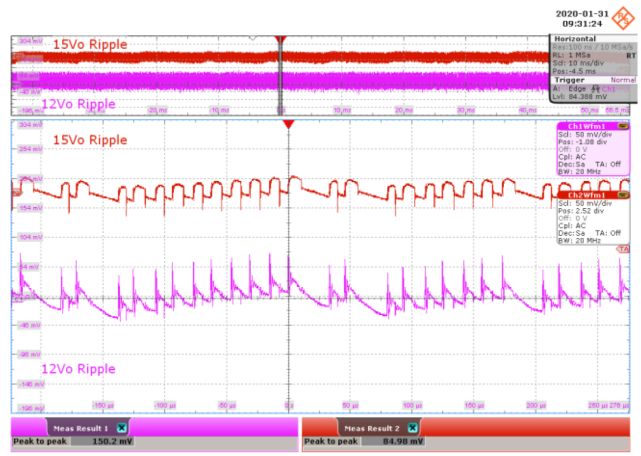

Figure 83 – 115 VAC 60 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 µs / div.
12 V Output Ripple = 150.2 mV.
15 V Output Ripple = 84.98 mV

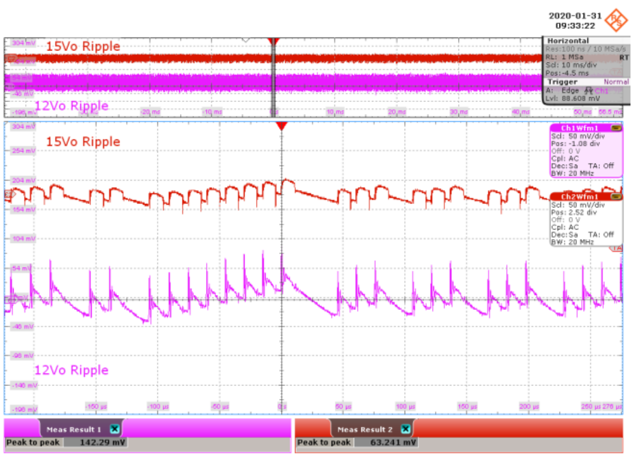

Figure 84 – 230 VAC 50 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 µs / div.
12 V Output Ripple = 142.29 mV.
15 V Output Ripple = 63.241 mV.

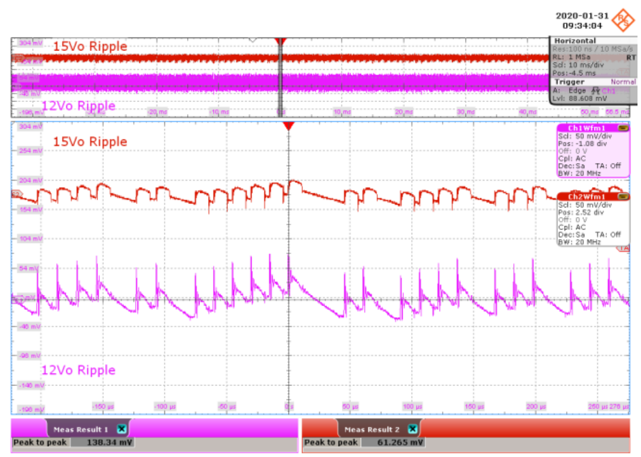

Figure 85 – 265 VAC 50 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 µs / div.
12 V Output Ripple = 138.34 mV.
15 V Output Ripple = 61.265 mV.

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11.5.2.2 75% Load Condition

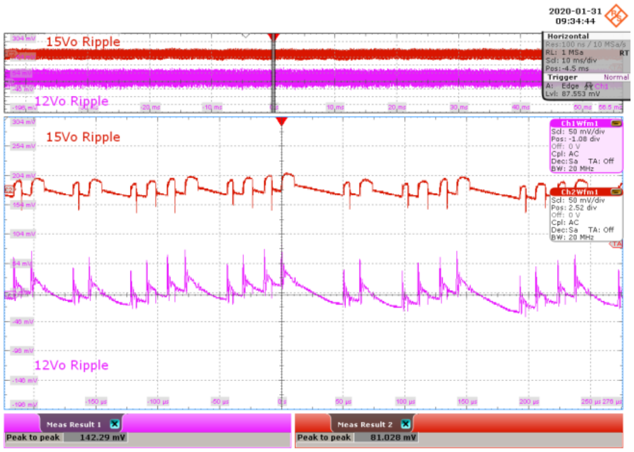

Figure 86 – 90 VAC 60 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 µs / div.
12 V Output Ripple = 142.29 mV.
15 V Output Ripple = 81.028 mV.

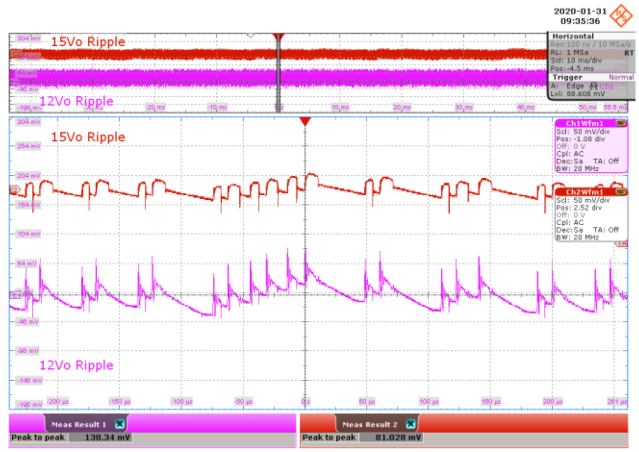

Figure 87 – 115 VAC 60 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 µs / div.
12 V Output Ripple = 138.34 mV.
15 V Output Ripple = 81.028 mV.

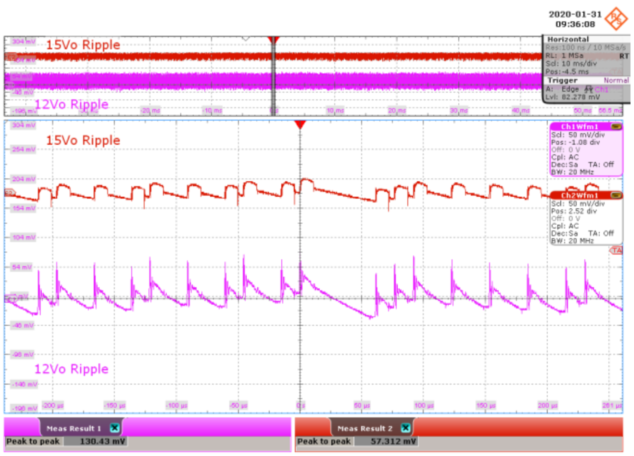

Figure 88 – 230 VAC 50 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 µs / div.
12 V Output Ripple = 130.43 mV.
15 V Output Ripple = 57.312 mV.

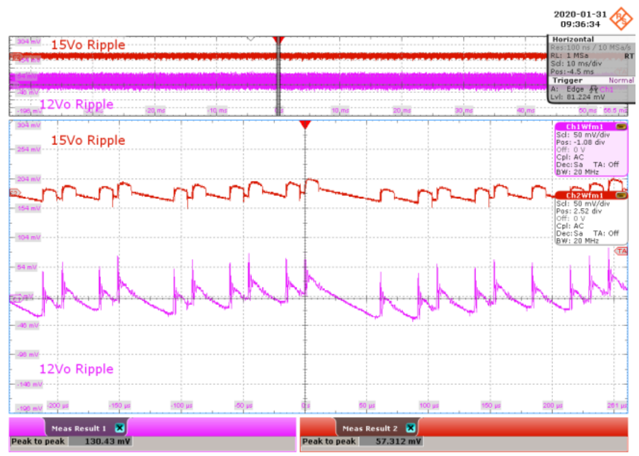

Figure 89 – 265 VAC 50 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 µs / div.
12 V Output Ripple = 130.43 mV.
15 V Output Ripple = 57.312 mV.

11.5.2.3 50% Load Condition

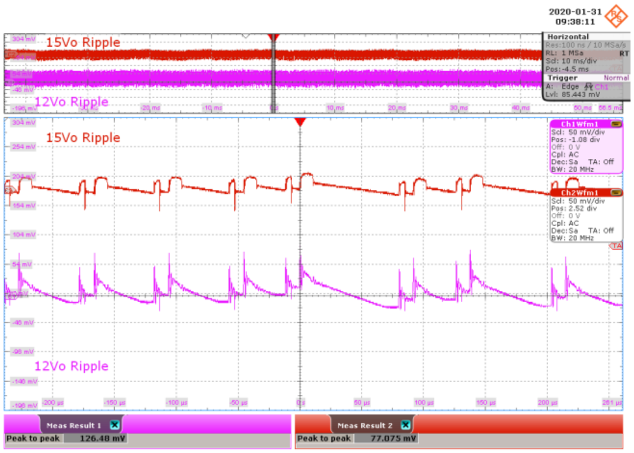

Figure 90 – 90 VAC 60 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 μs / div.
12 V Output Ripple = 126.48 mV.
15 V Output Ripple = 77.075 mV.

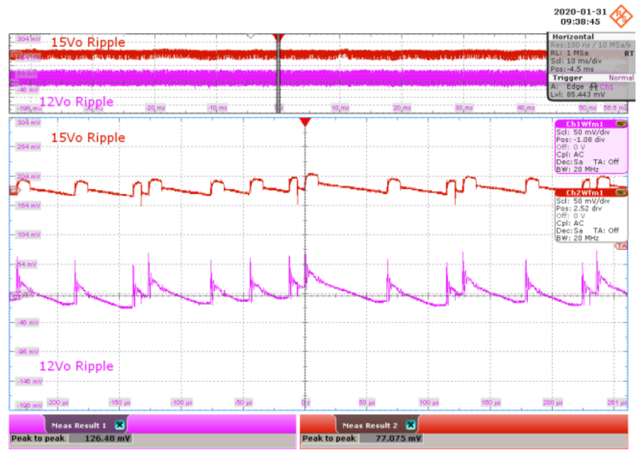

Figure 91 – 115 VAC 60 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 μs / div.
12 V Output Ripple = 126.48 mV.
15 V Output Ripple = 77.075 mV.

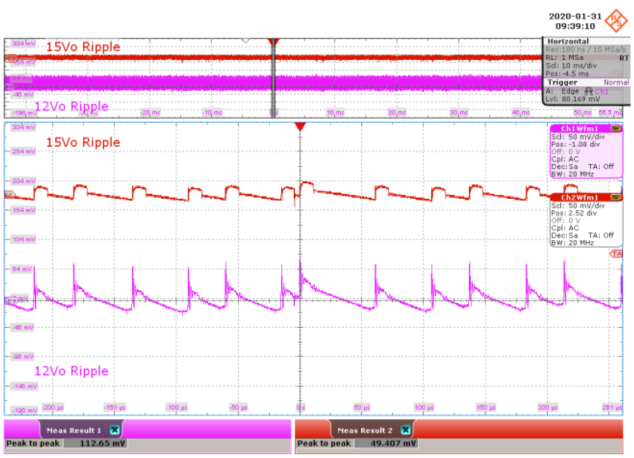

Figure 92 – 230 VAC 50 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 μs / div.
12 V Output Ripple = 112.65 mV.
15 V Output Ripple = 49.407 mV.

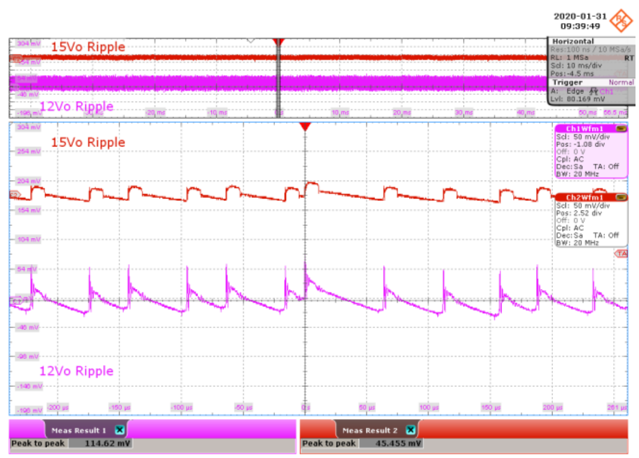

Figure 93 – 265 VAC 50 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 μs / div.
12 V Output Ripple = 114.62 mV.
15 V Output Ripple = 45.455 mV.

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11.5.2.4 25% Load Condition

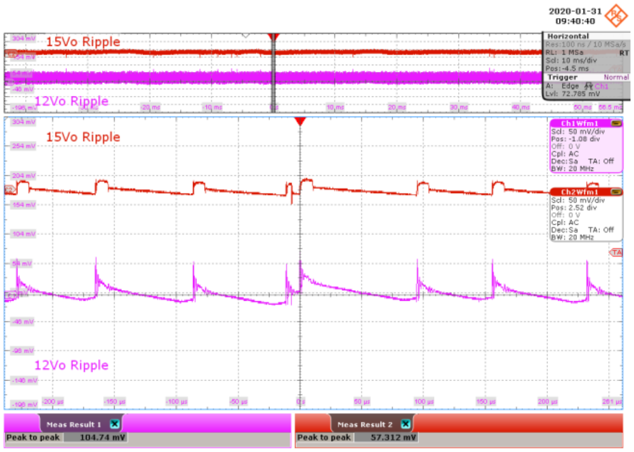

Figure 94 – 90 VAC 60 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 µs / div.
12 V Output Ripple = 104.74 mV.
15 V Output Ripple = 57.312 mV.

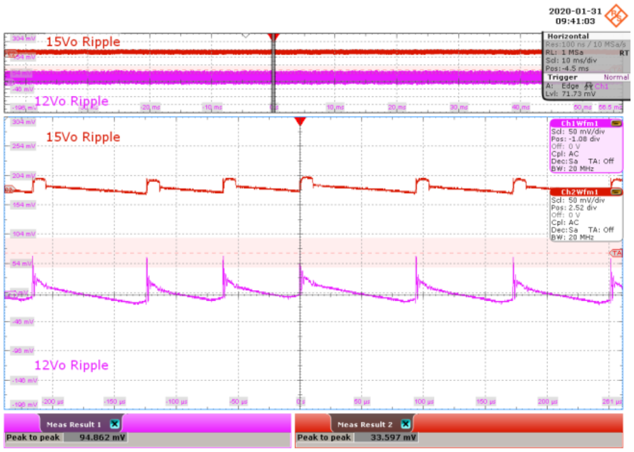

Figure 95 – 115 VAC 60 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 µs / div.
12 V Output Ripple = 94.862 mV.
15 V Output Ripple = 33.597 mV.

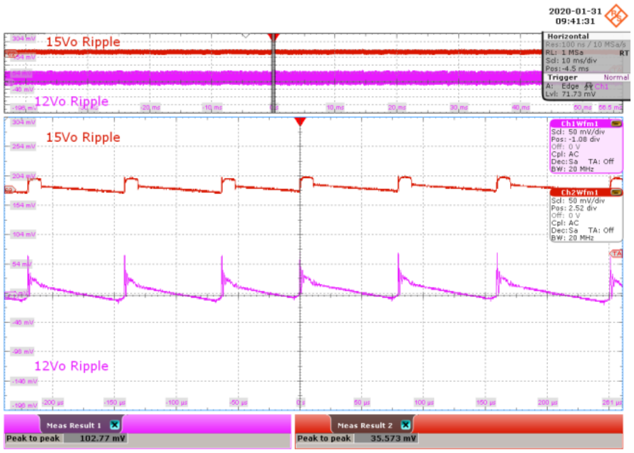

Figure 96 – 230 VAC 50 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 µs / div.
12 V Output Ripple = 102.77 mV.
15 V Output Ripple = 35.573 mV.

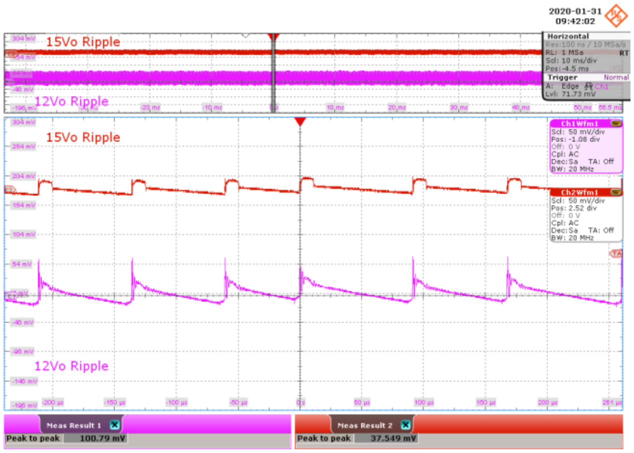

Figure 97 – 265 VAC 50 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 µs / div.
12 V Output Ripple = 100.79 mV.
15 V Output Ripple = 37.549 mV..

11.5.2.5 0% Load Condition

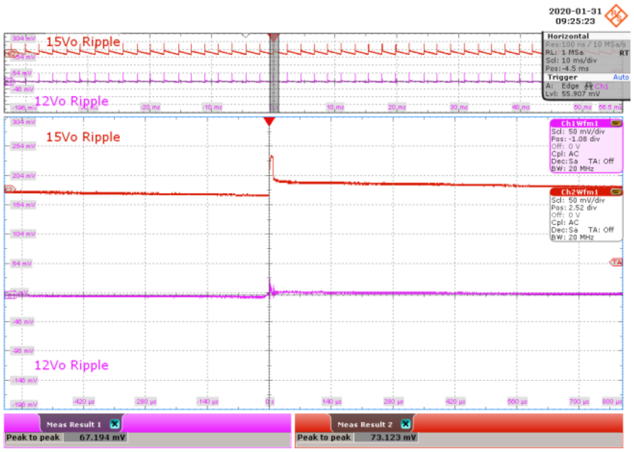

Figure 98 – 90 VAC 60 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 μs / div.
12 V Output Ripple = 67.194 mV.
15 V Output Ripple = 73.123 mV.

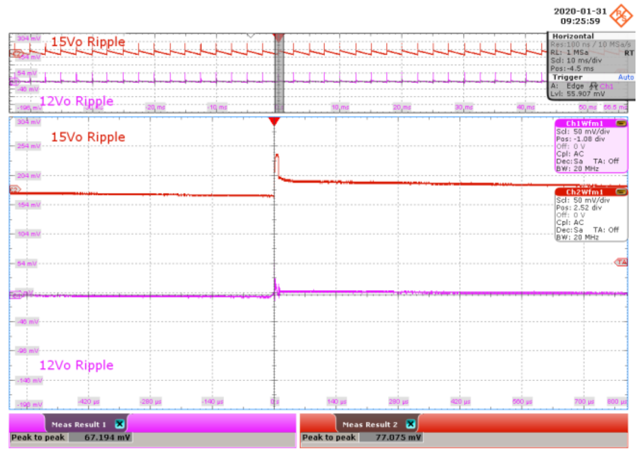

Figure 99 – 115 VAC 60 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 μs / div.
12 V Output Ripple = 67.194 mV.
15 V Output Ripple = 77.075 mV.

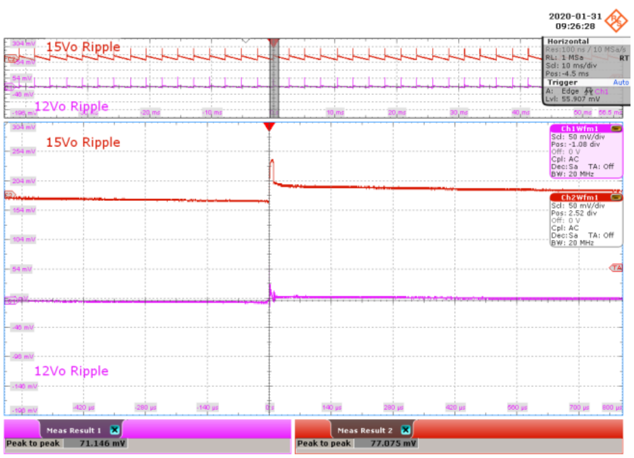

Figure 100 – 230 VAC 50 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 μs / div.
12 V Output Ripple = 71.146 mV.
15 V Output Ripple = 77.075 mV.

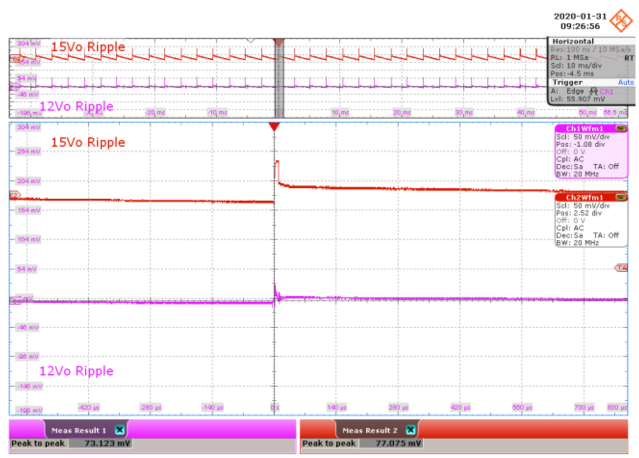

Figure 101 – 265 VAC 50 Hz.
CH1: V_{12V_OUT}, 50 V / div., 10 ms / div.
CH2: V_{15V_OUT}, 50 V / div., 10 ms / div.
Zoom: 50 μs / div.
12 V Output Ripple = 73.123 mV.
15 V Output Ripple = 77.075 mV.

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11.5.3 12 V Output Ripple Voltage Graph from 0% - 100%

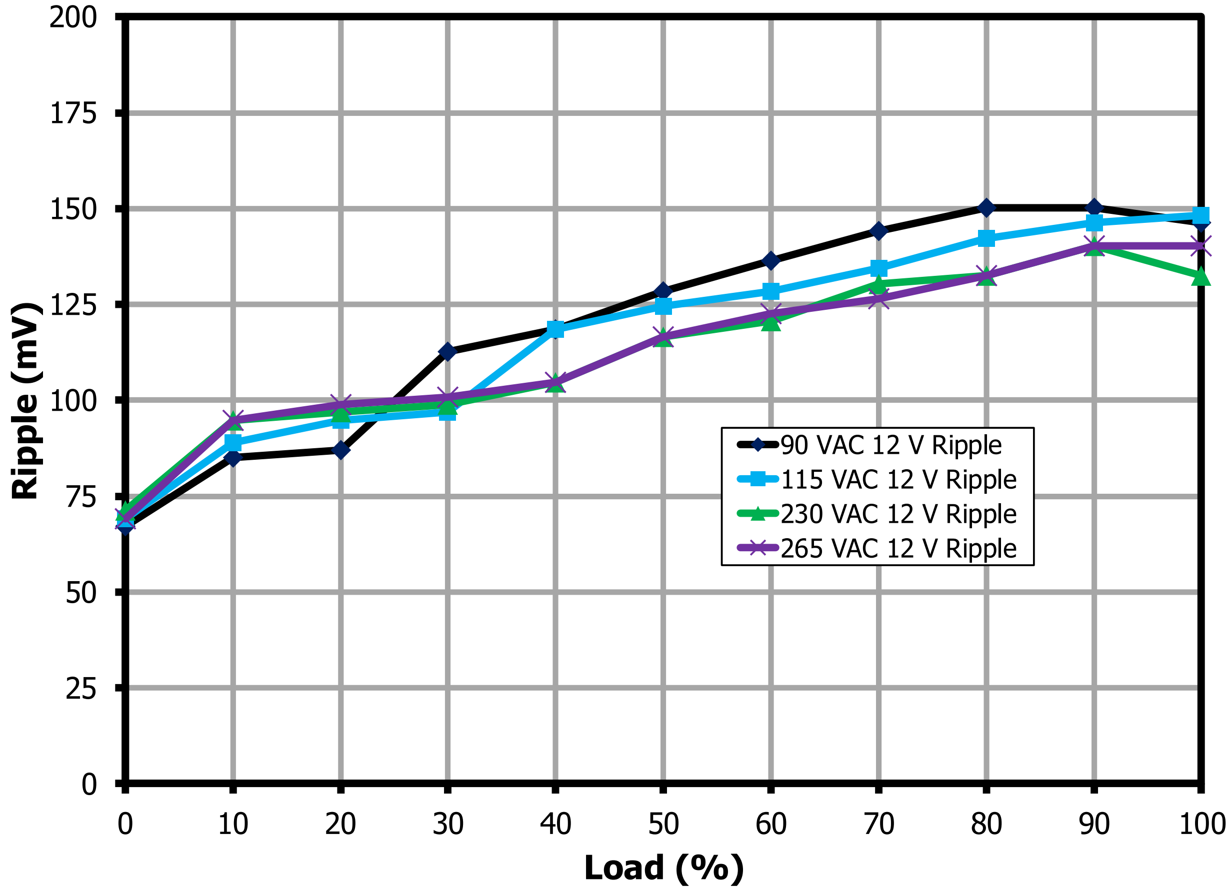

Figure 102 – 12 V Voltage Ripple (measured at PCB end at room temperature).

11.5.4 15 V Output Ripple Voltage Graph from 0% - 100%

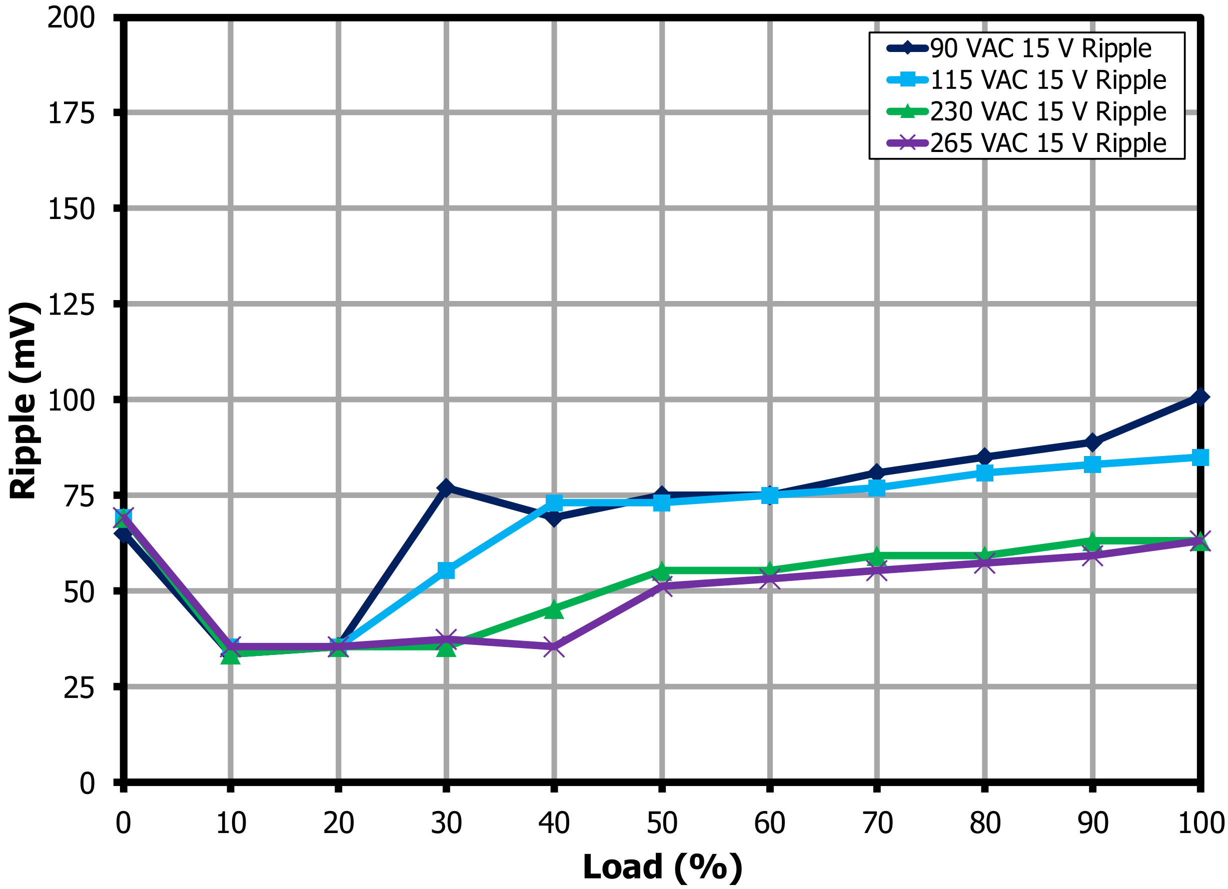

Figure 103 – 15 V Voltage Ripple (measured at PCB end at room temperature).

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12 Thermal Performance

12.1 *Test Set-Up*

Thermal evaluation was performed at room temperature with the circuit board enclosed inside an acrylic box. The circuit was soaked for one hour under full load conditions.

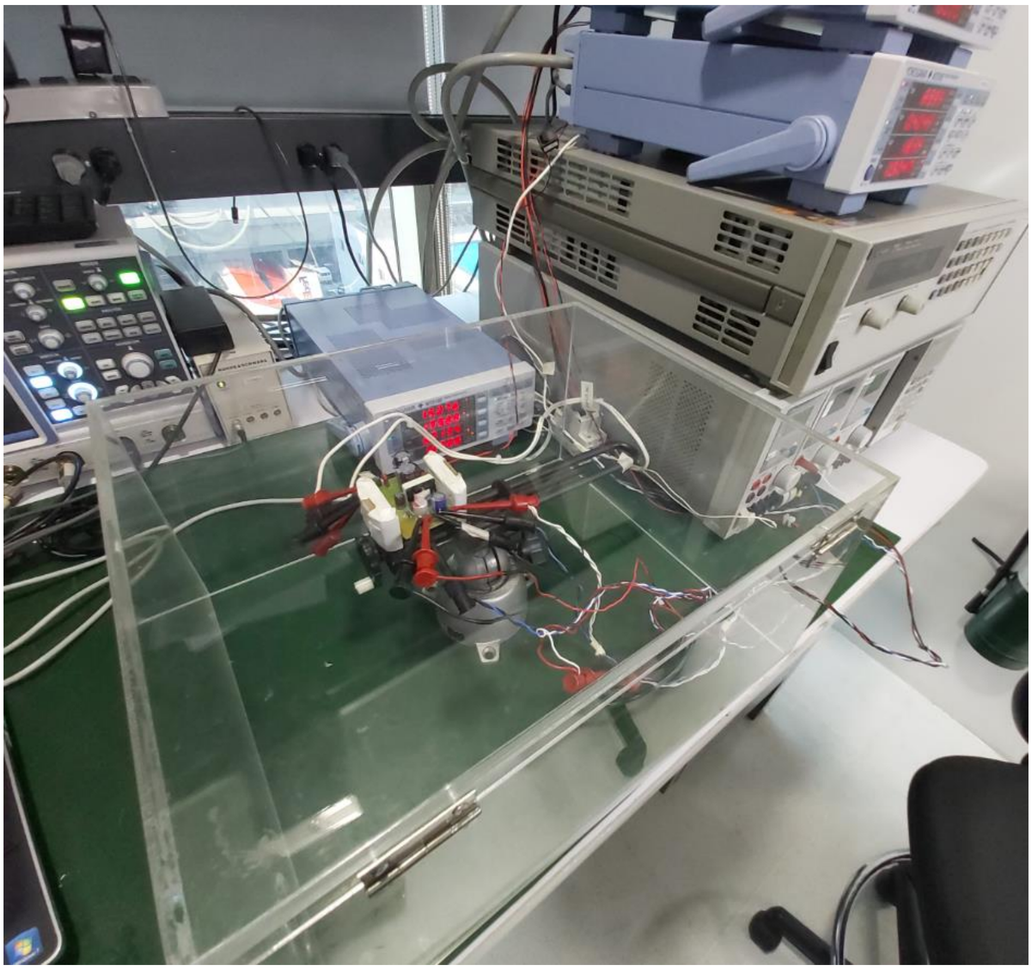
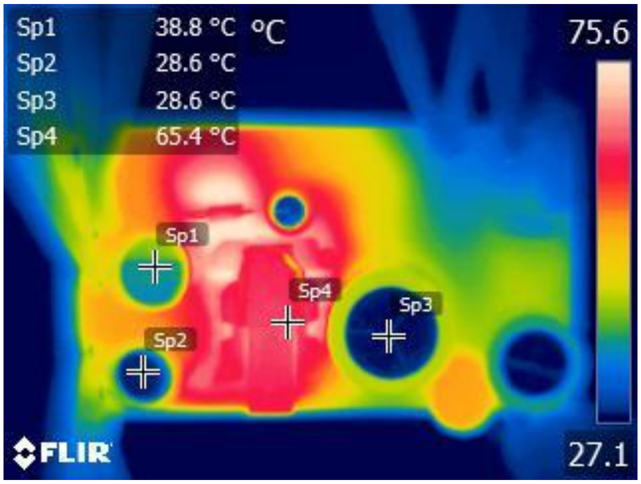


Figure 104 – Thermal Performance Set-up Using an Acrylic Box.

12.2 ***Thermal Performance at Room Temperature***

12.2.1 90 VAC at Room Temperature



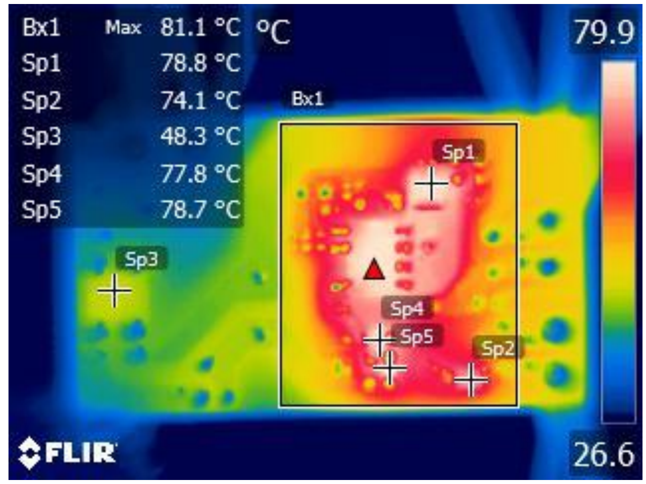


Figure 105 – Thermal Performance at 90 VAC.

Component	Temperature (°C)
Ambient	27.1
Input Capacitor (C9)	28.6
12V Output Capacitor (C11)	38.8
15V Output Capacitor (C8)	28.6
FreeWheeling Diode (D4)	78.8
LNK3206G (U1)	81.1
Transformer (T1)	65.4
Bridge (BR1)	48.3
Snubber Diode (D1)	77.8
Snubber Resistor (R10)	78.7
15V Diode (D3)	74.1

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12.2.2 265 VAC at Room Temperature

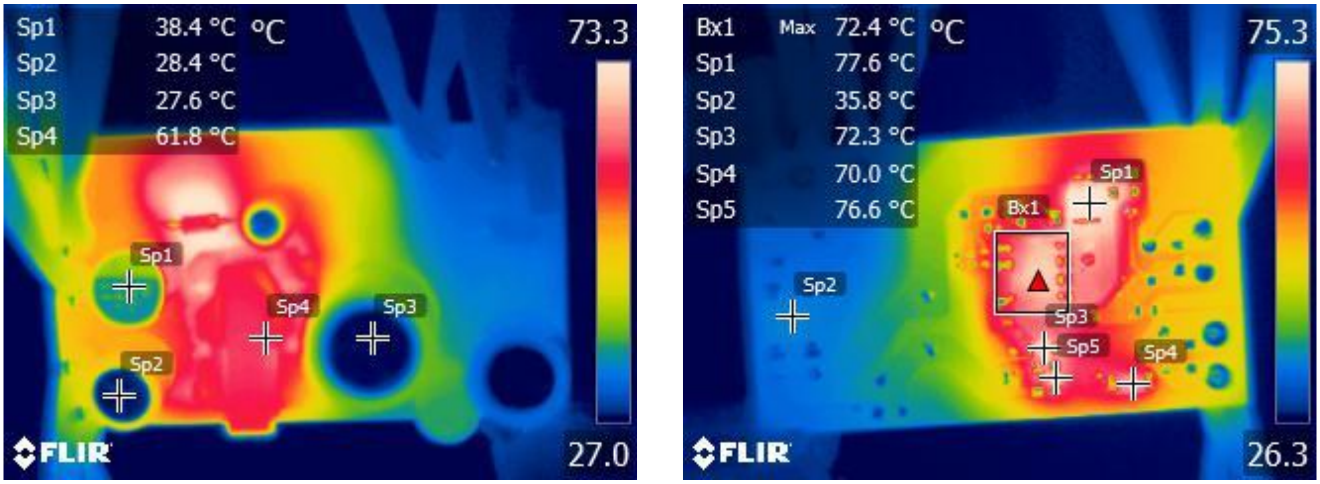

Figure 106 – Thermal Performance at 265 VAC.

Component	Temperature (°C)
Ambient	27.0
Input Capacitor (C9)	27.6
12V Output Capacitor (C11)	38.4
15V Output Capacitor (C8)	28.4
FreeWheeling Diode (D4)	77.6
LNK3206G (U1)	72.4
Transformer (T1)	61.8
Bridge (BR1)	35.8
Snubber Diode (D1)	72.3
Snubber Resistor (R10)	76.6
15V Diode (D3)	70.0

13 **Conducted EMI**

Conducted emissions tests were performed at 115 VAC and 230 VAC at full load (12 V 1 A, 15 V 0.2 A). Measurements were taken with floating ground.

13.1 ***Test Set-up Equipment***

13.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power Hi-tester.
4. Chroma measurement test fixture.
5. Input voltage set at 115 VAC and 230 VAC.
6. 12V RLOAD resistance is 12 ohms
7. 15V RLOAD resistance is 75 ohms

13.2 ***Test Set-up***

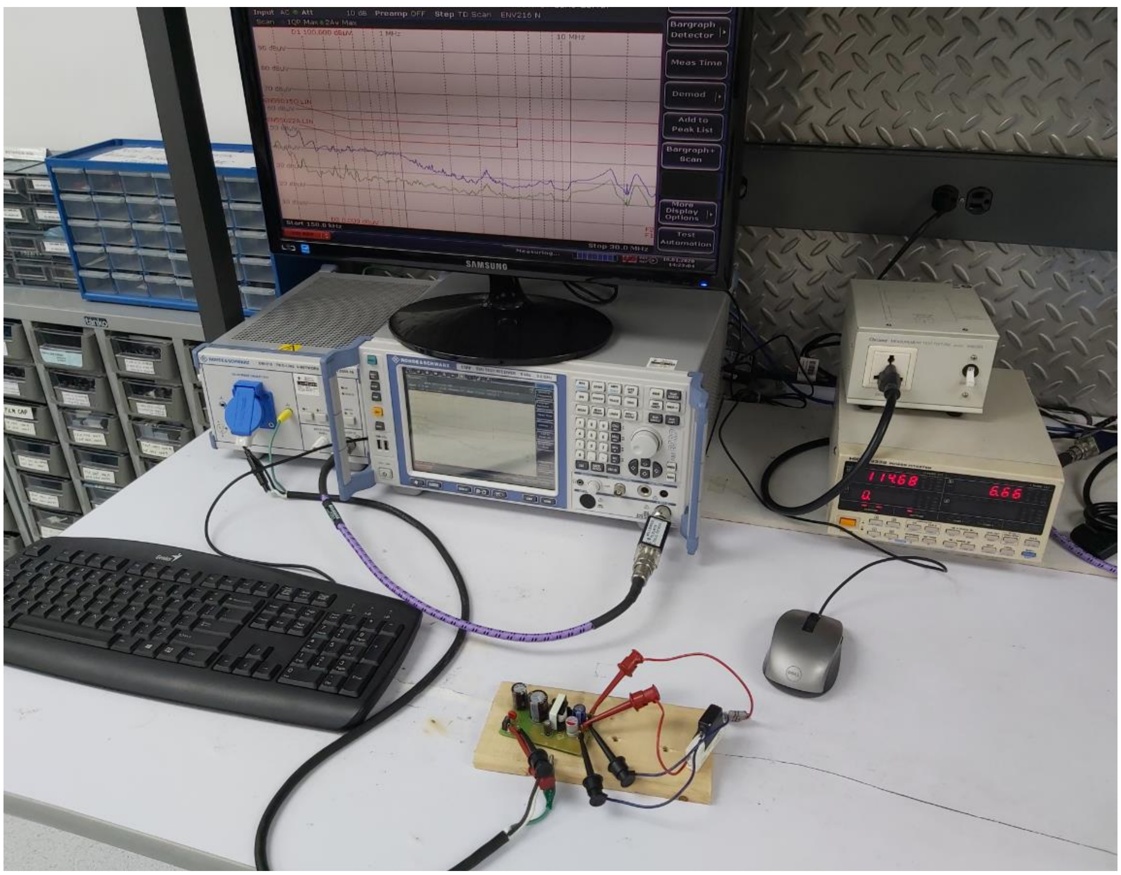

Figure 107 – EMI Test Set-up.

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13.3 ***Test Results***

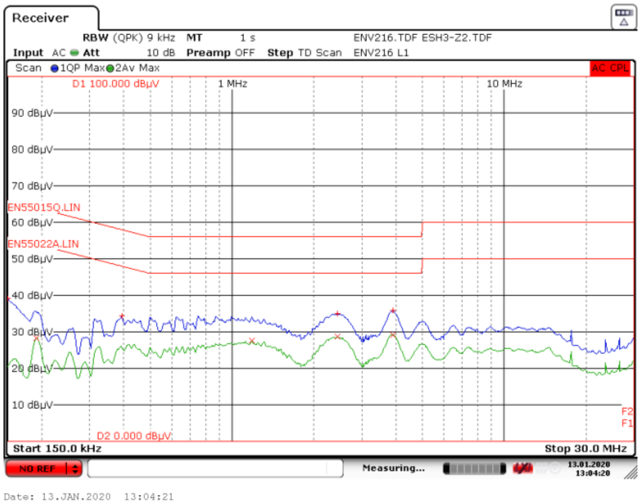

Figure 108 – 115 VAC 60 Hz.
Line with Floating Ground.

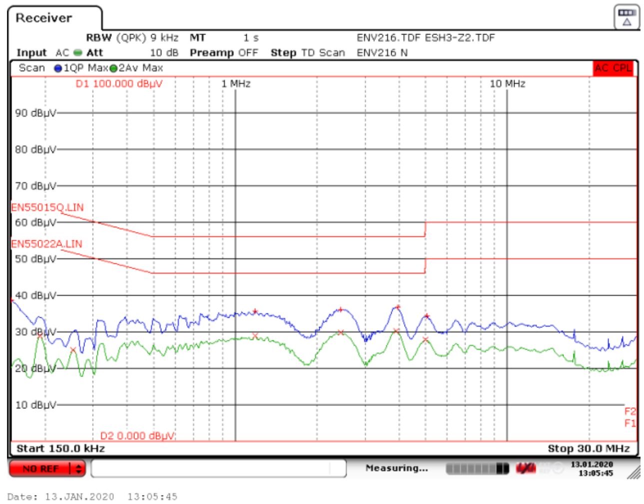

Figure 109 – 115 VAC 60 Hz.
Neutral with Floating Ground.

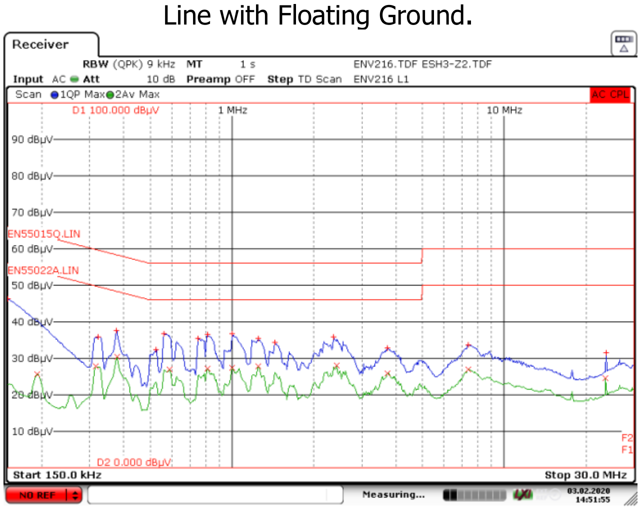

Figure 110 – 230 VAC 60 Hz.
Line with Output Grounded.

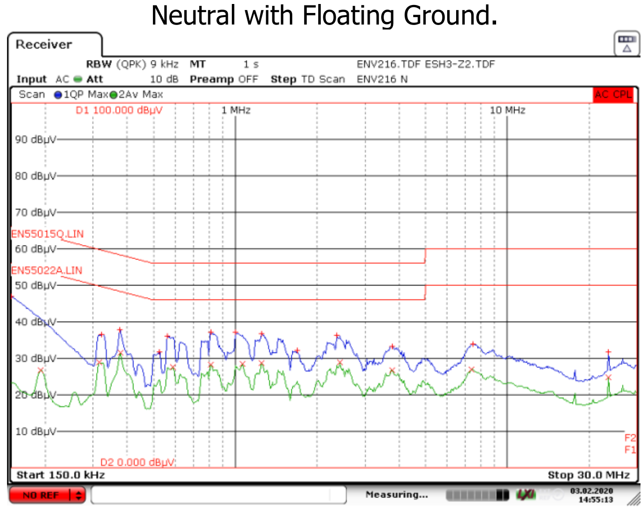

Figure 111 – 230 VAC 60 Hz.
Neutral with Output Grounded.

14 Line Surge

Differential mode input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

Differential Mode Surge

DM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1000	230	L to N	0	Pass
-1000	230	L to N	0	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass
+1000	230	L to N	180	Pass
-1000	230	L to N	180	Pass
+1000	230	L to N	270	Pass
-1000	230	L to N	270	Pass

Note: In all PASS results, no damage and no auto-restart was observed.

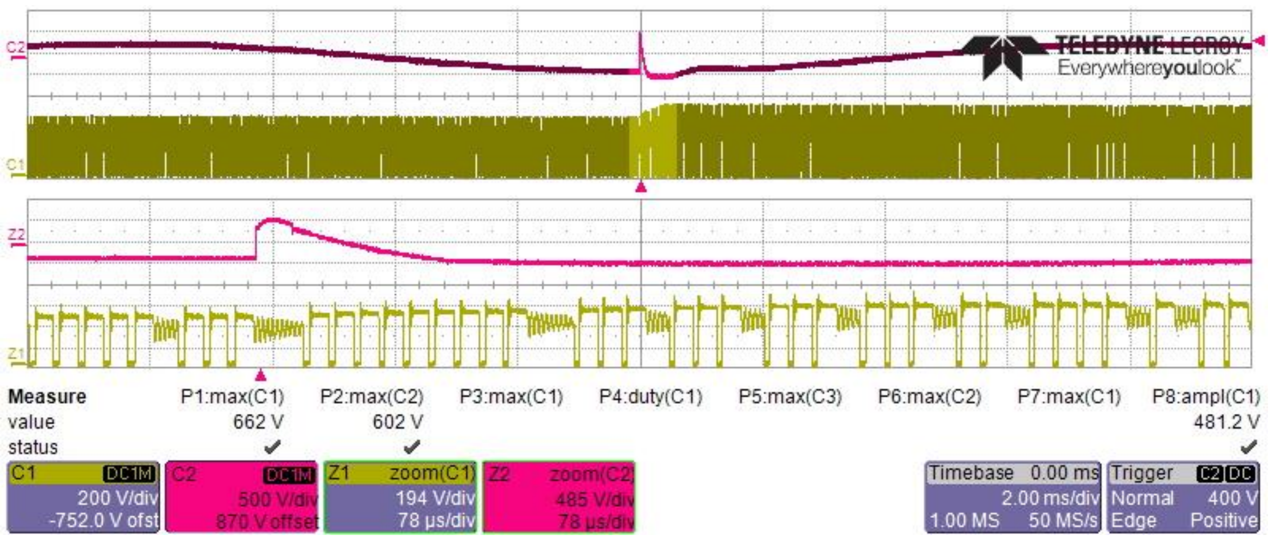

Figure 112 – Differential Mode Surge Input AC and V_{DS} waveform
Ch1: Vds 200 V / div., 2ms /div.
Ch2: Input AC 500 V / div., 2 ms / div.
Zoom: 78 μs / div.
$V_{DS(MAX)}$: 662 V.

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15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
26-Mar-20	RPA	1.0	Initial Release.	Apps & Mktg

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e-mail: usasales@power.com

CHINA (SHANGHAI)
Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

CHINA (SHENZHEN)
17/F, Hivac Building, No. 2, Keji
Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

GERMANY (AC-DC/LED Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

GERMANY (Gate Driver Sales)
HellwegForum 1
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@
power.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

ITALY
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

JAPAN
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

SINGAPORE
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

TAIWAN
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
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Phone: +44 (0) 7823-557484
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